1-1-2013

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10.1117/12.2022807

Wang, K., Nirmalathas, A., Lim, C., Skafidas, E., & Alameh, K. (2013). Free-space optics for high speed reconfigurable card-to-card optical interconnects. In Proceedings of SPIE: Nonimaging Optics: Efficient Design for Illumination and Solar Concentration X. Roland Winston, Jeffrey Gordon (Eds). Volume 8834 (pp. 88340I-1-88340I-6). San Diego, USA. SPIE.

Free-space optics for high-speed reconfigurable card-to-card optical interconnects

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ABSTRACT

High-speed card-to-card optical interconnects are highly demanded in high-performance computing and data centers. Compared with other solutions, free-space optical interconnects have the capability of providing both reconfigurability and flexibility. In this paper we propose and experimentally demonstrate a free-space based reconfigurable optical interconnect architecture and it is capable of connecting cards located both inside the same rack as well as in different racks. Results show that 3×10 Gb/s data transmission is achieved with a worst-case receiver sensitivity better than -9.38 dBm.

Keywords: Optical interconnects, free-space optical communication, reconfigurable optical interconnects.

1. INTRODUCTION

High-speed interconnects are highly demanded in data centers and high-performance computing and optical technologies have been proposed and widely studied to overcome the low-speed and high electro-magnetic interference bottlenecks of electrical interconnects [1]. For card-to-card optical interconnects, both multi-mode fiber (MMF) ribbons and polymer waveguides based architectures have been investigated [2, 3]. However, as the interconnect schemes used in the latter architectures are inherently point-to-point, free-space optics has been proposed for dynamically interconnecting cards, thus offering better flexibility for efficient operation [4].

In previous studies, we have experimentally demonstrated a reconfigurable card-to-card optical interconnect architecture using MEMS-based steering mirrors for efficient link reconfiguration [5]. However, the achievable interconnection range was highly limited due to the Gaussian beam divergence while propagating in the free-space and only cards located inside the same rack can be connected. In this paper, we show that by using hybrid free-space and MMF signal propagation, cards both inside the same rack and in different racks can be connected. Experimental results show that 3×10 Gb/s data transmission is achieved with a receiver sensitivity (at the bit-error-rate (BER) of 10^{-9}) better than -9.38 dBm.

2. PROPOSED SYSTEM ARCHITECTURE

The architecture of proposed reconfigurable optical interconnect is shown in Fig. 1 [5]. A dedicated optical interconnect module is integrated onto each electronic card (typically a PCB) and inside the module a VCSEL array is used in conjunction with a collimating lens array to generate digitally-modulated collimated Gaussian optical beams. A MEMS-based transmitter mirror array is employed to adaptively steer the optical beams to various destinations, thus providing interconnect reconfigurablity and operation flexibility. After propagating in free-space, at the receiver side the modulated optical signals are appropriately steered with another receiver MEMS mirror array and focused onto the corresponding photodiodes (PD) elements.

To connect cards located in different racks, a rack gateway is proposed to be integrated onto each rack, which consists of MEMS steering mirrors and MMF collimators. Through appropriate beam steering, the optical signal is coupled to a MMF collimator and transmitted to the destination rack. At the receiver side, the modulated optical signal exiting the

MMF collimator is appropriately steered by another MEMS mirror element and focused onto the corresponding PD element.

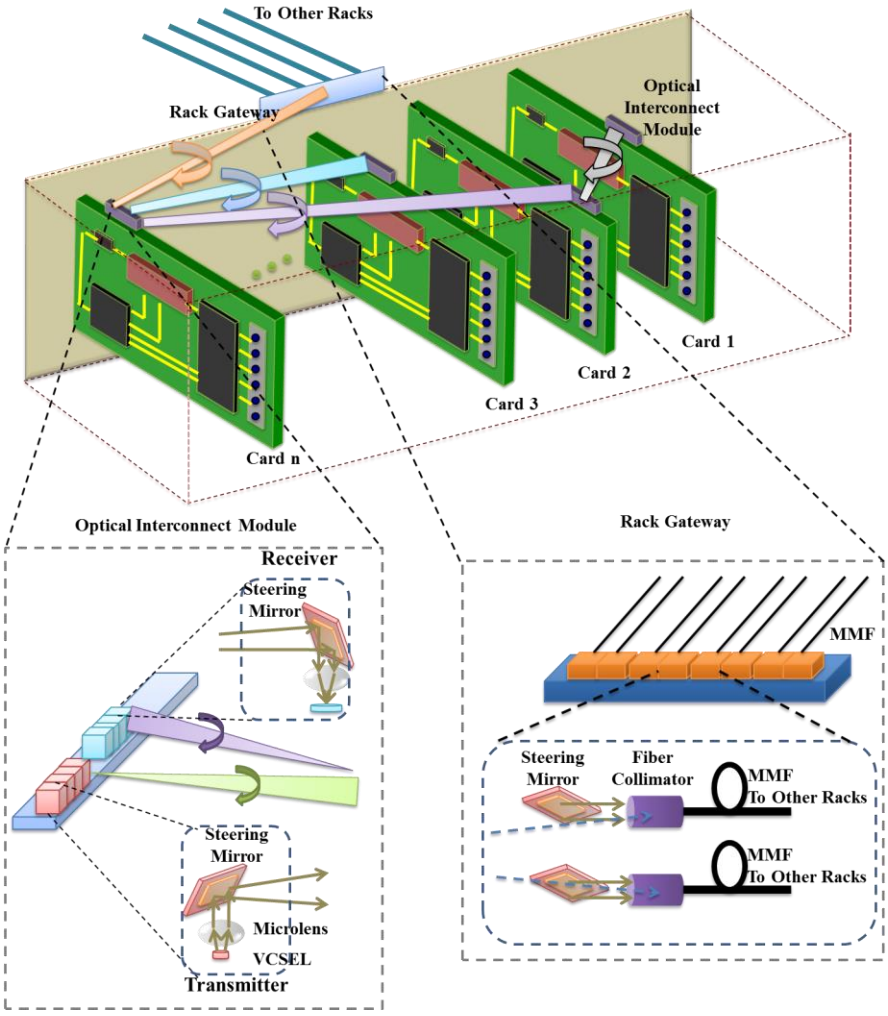


Figure 1. Proposed reconfigurable card-to-card optical interconnect architecture capable of connecting cards located both inside the same rack and in different racks.

3. EXPERIMENTS AND DISCUSSIONS

Experiments were carried out to demonstrate the proposed reconfigurable optical interconnect architecture for connecting cards located both inside the same rack and in different racks using the setup shown in Fig. 2. PCB based integrated optical interconnect modules were designed and fabricated. Specifically, a 1×4 VCSEL array (850 nm, ~17^{o} divergence angle and 250 μm pitch), the corresponding VCSEL driver circuits (4 QFN packaged drivers), a 1×4 PD array (60 μm active diameter, 250 μm pitch and ~0.6 A/W responsivity at 850 nm) and 4 trans-impedance amplifier (TIA) chips were integrated onto a single small-size PCB. A micro-lens array (250 μm pitch with ~236 μm clear aperture) was then aligned and mounted on top of the VCSEL array and the PD array to collimate the VCSEL beams and focus received optical beams onto the active windows of the PD elements. Each of the micro-lens arrays was attached to

an XYZ translational stage, and the distance between the VCSEL/PD plane and the lens was changed manually (equal to the focal length). Separate MEMS steering mirror chips (<5 ms point-to-point switching time) were used to switch the optical beams to the various receiving cards. The MEMS mirror chips were attached to XYZ translational stages and dynamically steered by changing the voltage applied to their activators. In addition, the size of the MEMS mirror was larger than the pitch of the VCSEL and PD arrays, so only three out of the four available channels were used (the third VCSEL and PD elements were not used).

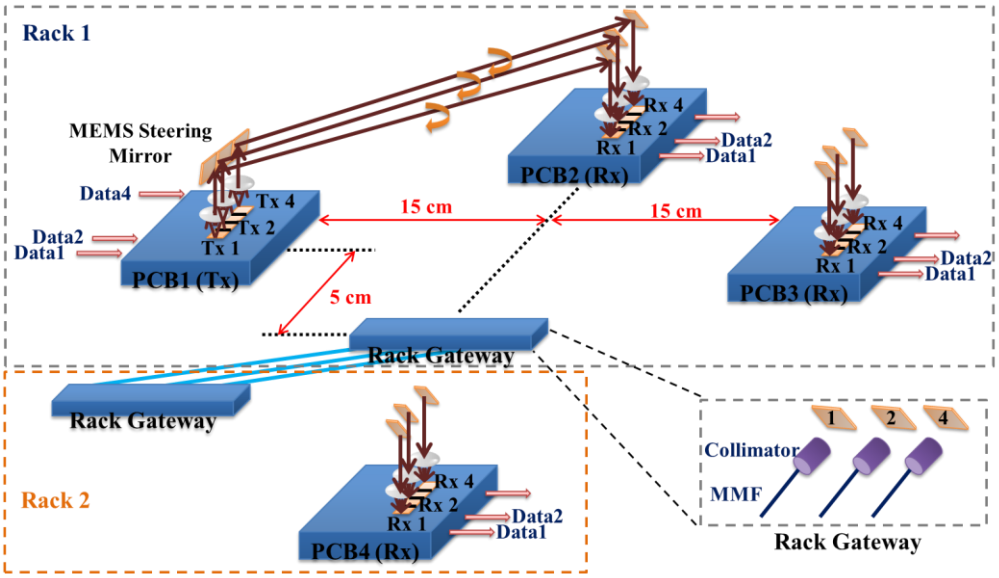
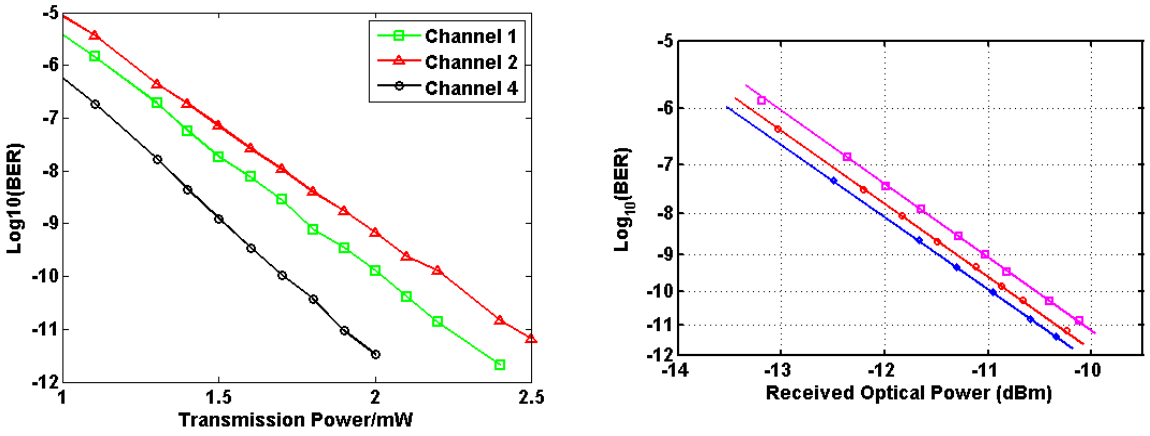


Figure 2. Experimental setup to demonstrate the proposed free-space based reconfigurable card-to-card optical interconnect architecture.

To connect cards located in different racks, the signals were appropriately steered to the rack gateway, which consisted of fiber collimators (3 used in the experiment). After propagating in the MMFs, the exiting signals were then guided to the final destination card. In front of the MMF collimators, MEMS steering mirrors were also employed to minimize the incident angles for maximum coupling efficiency or to guide the signals for detection.

Four integrated optical interconnect modules and two rack gateways were used in the proof-of-concept experiment and the distances between modules located inside the same rack were shown in Fig. 2. The rack gateways were connected with 10 m MMFs (62.5 μm). The MMF collimators had a return loss of >18 dB and a total diameter of 5 mm, and the distance between adjacent collimators was chosen to be 10 mm. In addition, during the measurements, the bit rate for each channel was set to 10 Gbps and on-off-keying (OOK) modulation was used (2^{31}-1 PRBS data).

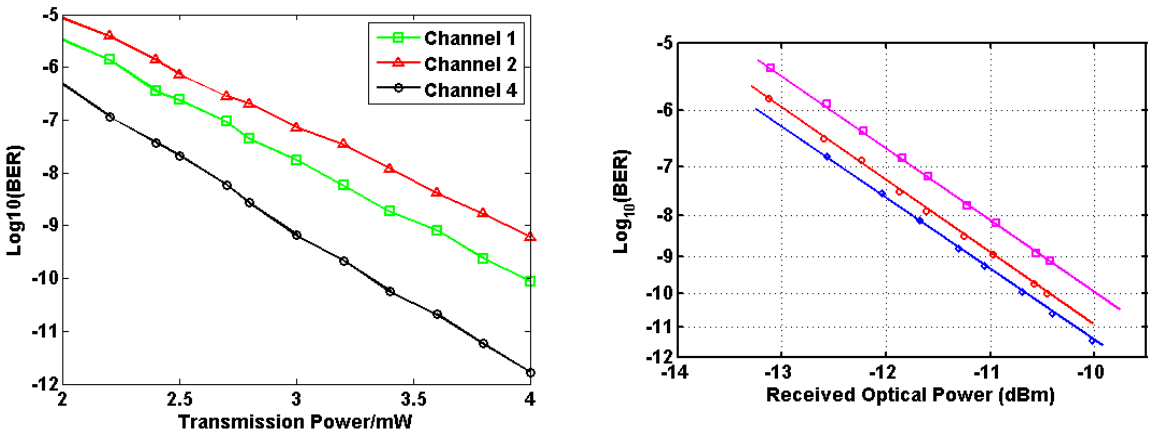
To demonstrate the concept of the proposed optical interconnect architecture, module 1 was first connected to module 2 and inside the modules, VCSEL element n (n=1, 2, and 4) sent data to PD element n. The measured bit-error-rate (BER) versus the VCSEL power is shown in Fig. 3 (a). It is clear that with the same optical power, the BER performance for channel 2 is worse than the performances of the other channels. This is mainly due to larger inter- channel crosstalk since PD element 2 is in the center of the array. Fig. 3 (b) shows the measured BER versus the received optical power (obtained by changing the output powers of the VCSEL elements) for the three working channels. It can be seen that channel 4 has the best receiver sensitivity while the sensitivity for channels 2 is the worst. These results are consistent with the results shown in Fig. 3(a).



(a) (b)

Figure 3. Measured BER versus (a) VCSEL power and (b) received power. Optical interconnect module 1 connected to module 2.

To demonstrate the reconfigurability and flexibility of proposed interconnect scheme, a second scenario was considered where module 1 was interconnected with module 3. The measured BER versus transmitted optical power and the receiver sensitivity are shown in Fig. 4(a) and Fig. 4 (b), respectively. It can be seen that a BER much better than 10^{-9} is achieved. Furthermore, it is clear that with the same transmission power, the BER performances for all three channels shown in Fig. 4 (a) are worse than those shown in Fig. 3(a). This can be attributed to the longer free-space propagation distance and the Gaussian beam divergence, which result in smaller received signal power and larger crosstalk. This observation can be further confirmed by comparing the results shown in Fig. 4(b) and Fig. 3(b), where the receiver sensitivity is slightly degraded.

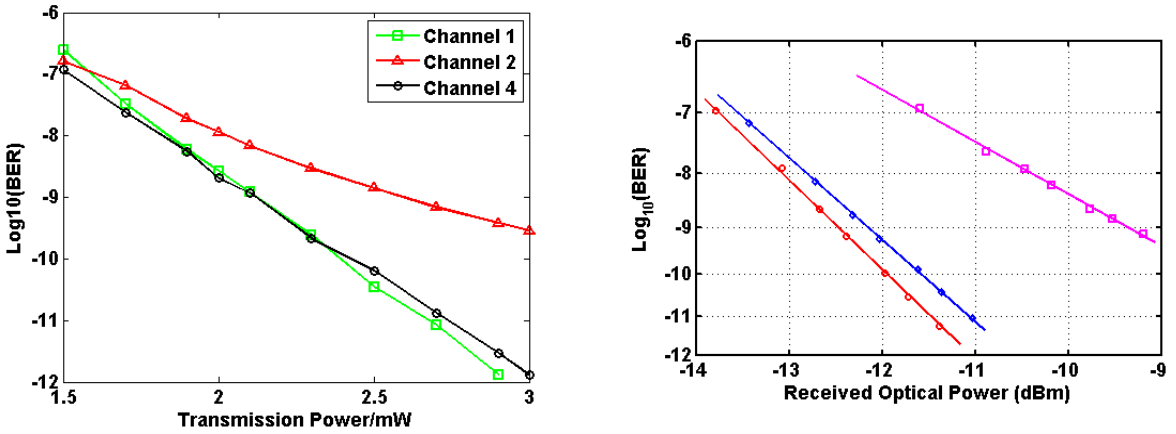


(a) (b)

Figure 4. Measured BER versus (a) VCSEL power and (b) received power. Optical interconnect module 1 connected to module 3.

Experiments were also carried out to demonstrate the feasibility of proposed system architecture to connect cards in different racks. Here the signals were steered to the rack gateway and after being coupled into and propagating inside MMFs, they were detected with optical interconnect module 4. The free-space transmission distance between rack

gateway 2 and module 4 was 4 cm. The BER performance versus VCSEL power and the receiver sensitivity are shown in Fig. 5 (a) and Fig. 5(b), respectively. Comparing with previous results, channel 2 in this scenario has much worse performance than the performances of the other channels. This is mainly due to the fact that inter-channel crosstalk signals are also coupled into the channel 2 MMF, and that the MEMS mirror at the receiver side cannot steer them out of the active window of corresponding PD element. Figs 3-5 demonstrate the capability of the proposed reconfigurable optical interconnect architecture to achieve 3×10 Gb/s data transmission with a worst-case receiver sensitivity better than -9.38 dBm.



(a) (b)

Figure 5. Measured BER versus (a) VCSEL power and (b) received power. Optical interconnect module 1 connected to module 4.

4. CONCLUSIONS

In this paper, we have proposed and experimentally demonstrated a reconfigurable optical interconnect architecture capable of connecting cards located both inside the same rack and in different racks. 3×10 Gb/s data transmission has been experimentally achieved and the worst-case receiver sensitivity has been shown to be better than -9.38 dBm.

ACKNOWLEDGEMENT

This work was supported in part by NICTA and by the Department of Industry, Innovation, Science, Research and Tertiary Education (DIISRTE). NICTA is funded by the Australian Government as represented by the Department of Broadband, Communications and the Digital Economy and the Australian Research Council through the ICT Excellence Program.

REFERENCES

[1] A. F. Benner, M. Ignatowski, J. A. Kash, D. M. Kuchta, and M. B. Ritther, “Exploitation of optical interconnects in future server architectures,” IBM J. Res. Develop., vol. 49, no. 4.5, pp. 755-775, Jul. 2005.

[2] F. E. Doany, B. G. Lee, A. V. Rylyakov, D. M. Kuchta, C. Baks, C. Jahnes, F. Libsch, and C. L. Schow, “Terabit/sec VCSEL-based parallel optical module based on holey CMOS transceiver IC” in Proc. Optical Fiber

Communication Conference and Exposition and the National Fiber Optic Engineers Conference (OFC/NFOEC), Los Angeles, California, 2012, pp. PDP5D.9.

[3] C. L. Schow, F. E. Doany, C. W. Baks, Y. H. Kwark, D. M. Kuchta, and J. A. Kash, "A single-chip CMOS-based parallel optical transceiver capable of 240-Gb/s bidirectional data rates" J. Lightw. Technol. 27, 915-929 (2009).

[4] M. Aljada, K. E. Alameh, Y. T. Lee, and I. S. Chung, "High-speed (2.5 Gbps) reconfigurable inter-chip optical interconnects using opto-VLSI processors," Opt. Express, vol. 14, no. 15, pp. 6823–6836, July 2006.

[5] K. Wang, A. Nirmalathas, C. Lim, E. Skafidas, and K. Alameh, "Experimental demonstration of high-speed free-space reconfigurable card-to-card optical interconnects," Opt. Express, vol. 21, pp. 2850-2861, 2013.