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A novel reconfigurable optical interconnect architecture using an Opto-VLSI processor and a 4-f imaging system

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Abstract: A novel reconfigurable optical interconnect architecture for on-board high-speed data transmission is proposed and experimentally demonstrated. The interconnect architecture is based on the use of an Opto-VLSI processor in conjunction with a 4-f imaging system to achieve reconfigurable chip-to-chip or board-to-board data communications. By reconfiguring the phase hologram of an Opto-VLSI processor, optical data generated by a vertical Cavity Surface Emitting Laser (VCSEL) associated to a chip (or a board) is arbitrarily steered to the photodetector associated to another chip (or another board). Experimental results show that the optical interconnect losses range from 5.8dB to 9.6dB, and that the maximum crosstalk level is below −36dB. The proposed architecture is tested for high-speed data transmission, and measured eye diagrams display good eye opening for data rate of up to 10Gb/s.

OCIS codes: (060.6718) Switching, circuit.

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1. Introduction

In advanced high performance computing (HPC) systems, the increasing demand for high-speed processing capability will require high-speed optical interconnects in order to overcome the limited bandwidth and electromagnetic interference (EMI) bottlenecks of electrical interconnects [1]- [4]. Electrical interconnects have high failure probability, especially at computing nodes such as processors, memories and input/output ports [5]- [6]. In addition to removing the bottlenecks of electrical interconnects, optical interconnect technologies offer a large number of interconnect channels, integration and reconfigurability [1] [6]- [9]. Recent reports by both academia and industry have predicted that the electrical interconnect technology will be replaced by optical interconnect technologies for high performance computing in the next decade [1] [5] [10]. Different approaches for signal transmission and distribution have recently been reported, including, polymer waveguides [11]- [12], fiber ribbons [13]- [14], fiber image guides [15]- [16], and free space optical interconnects using lenses and mirror systems [17]- [21].

Among the various reported optical interconnect architectures, the free-space optical interconnect is a promising solution to achieving large bandwidth and low power consumption while keeping other advantages of low losses and EMI performances for HPC data communication links. Free-space optical interconnects enable dense and reconfigurable optical signal transmission and distribution to be realized simultaneously. A reconfigurable free space optical interconnect architecture, employing a liquid crystal on silicon (LCoS) processor in conjunction with a polarization beam splitter, has been reported [17], demonstrating an optical loss of 13.6dB and a bit error rate (BER) of 10^{-12} at 1.25Gb/s. Another reconfigurable optical interconnect architecture based on the use of a prism together with a lens and a spatial light modulator (SLM) has also been adopted [22]. A 2.5Gb/s reconfigurable optical interconnect architecture constructed using two Opto-very-large-scale-integration (Opto-VLSI) processors has been reported, demonstrating experimentally the ability of Opto-VLSI processors to realise free-space point-to-point as well as point-to-multi-point optical interconnects [23].

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In this paper, we propose and experimentally demonstrate a novel fiber-based optical interconnect architecture based on the use of an Opto-VLSI processor in conjunction with a 4-f imaging system, where the input optical beams carrying data from VCSEL transmitters can be steered and arbitrarily switched to different output fiber ports (or receivers). The proposed reconfigurable optical interconnect architecture can realize chip-to-chip or board-to-board communication at data rates of up to 10Gb/s.

2. Opto-VLSI processor

The Opto-VLSI processor is a core element used in the proposed optical interconnect architecture. It consists of Very-Large-Scale-Integrated (VLSI) circuits that drive an array of liquid crystal (LC) cells [24]. It can generate multi-phase holographic blazed gratings capable of steering or shaping optical beams, as illustrated in Fig. 1. Each pixel of the Opto-VLSI processor is independently driven by a discrete voltage applied between the aluminum mirror

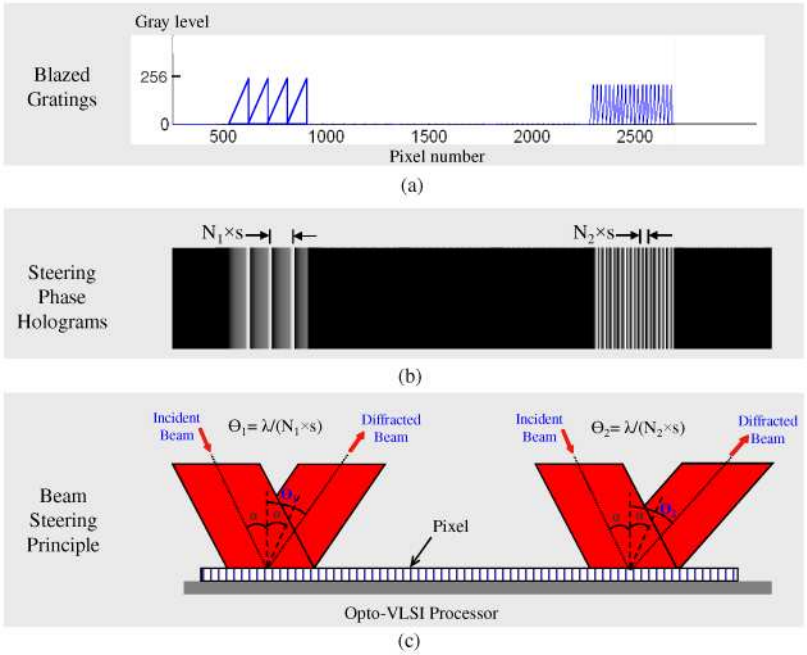

Fig. 1. (a) Gray level versus pixel number of different blazed gratings; (b) Corresponding computer-generated steering phase holograms; (c) Principle of beam steering using an Opto-VLSI processor. The steering angle is inversely proportional to the blazed grating period.

electrode across the LC cells and a transparent Indium-Tin oxide (ITO) layer as the second electrode. A quarter-wave-plate (QWP) layer between the LC and the aluminum mirror is usually used to accomplish polarization-insensitive operation [25].

An Opto-VLSI processor is electronically controlled, software configurable and is capable of controlling multiple optical beams simultaneously without mechanical moving parts. For an optical beam incident on an Opto-VLSI processor with a small incidence angle, the x-direction θ_x or the y-direction θ_y of the 1st-order diffraction beam is determined by the linearized grating equation [26]:

$$\theta_{x/y} = \frac{\lambda}{p_{x/y}} = \frac{\lambda}{(s_{x/y})(N_{x/y})} \tag{1}$$

where $p_{x/y}$ is grating period in the x-direction or the y-direction, $s_{x/y}$ is the size of square or rectangular liquid crystal pixels and $N_{x/y}$ is the number of the pixels in a period of the grating.

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The digitized phase levels, $\{\varphi_n\}$, and steering efficiency $\eta(M)$ of the grating can be expressed as:

$$\phi_n = n\frac{2\pi}{M}, \quad n = 1,...,M \tag{2}$$

and

$$\eta(M) = \left[\frac{\sin(\pi/M)}{(\pi/M)}\right]^2 \tag{3}$$

where M is the number of discrete phase levels. Equation (1) shows that a diffracted beam can be steered to a desired direction $\theta_{x/y}$ by selecting $p_{x/y}$ parameters i.e. $s_{x/y}$ and $N_{x/y}$ for a certain wavelength. The steered beam intensity (or steering efficiency) is dependent on the number of discrete phase levels as shown in Eq. (3).

3. Proposed reconfigurable optical interconnect architecture

Figure 2 shows the proposed reconfigurable optical interconnect architecture. The principle of operation is illustrated through an example of a reconfigurable optical interconnect architecture providing interconnections between a set of three chips (Chips 1-3) and another set of three chips (Chips 4-6). Each chip of a set is associated with a VCSEL device that is modulated by the data generated by that chip, and three photodetectors (PDs) that receive data from the three different chips that belong to the other set. The output optical beam of a VCSEL element is coupled into an optical fiber connected to a 1x3 optical switch, implemented using an Opto-VLSI-based 4-f imaging system, as will be illustrated subsequently. The output fiber ports of the optical switches of a set are connected to the photodetectors associated with the chips of the other set, as illustrated in Fig. 2. The outputs of the photodetectors linked to a chip are connected to the receiving data port of that chip. In this way, the interconnection between two chips is mainly controlled by the Opto-VLSI switch. Figure 3 illustrates the Opto-VLSI processor and the 4-f imaging system used to implement the optical switches required for the reconfigurable optical interconnect architecture in Fig. 2. A lens, of focal length *f*, which collimates the divergent optical beam from the input optical fiber associated to a VCSEL element, is placed at a distance *f* from the fiber array. The vertical spacing between the input fiber and the optical axis of the lens is around a quarter of the fiber array spacing (250 μm). The collimated beam incident on the active window of the Opto-VLSI processor, which is placed at a distance *f* from the lens, can be steered to any of the three fiber ports, associated to the lens, using phase holograms (or blazed gratings) uploaded onto the Opto-VLSI processor, as illustrated in Fig. 1. Note that several 1x3 switches can be realized using a single Opto-VLSI processor partitioned into several pixel blocks that are independently driven by appropriate steering phase holograms.

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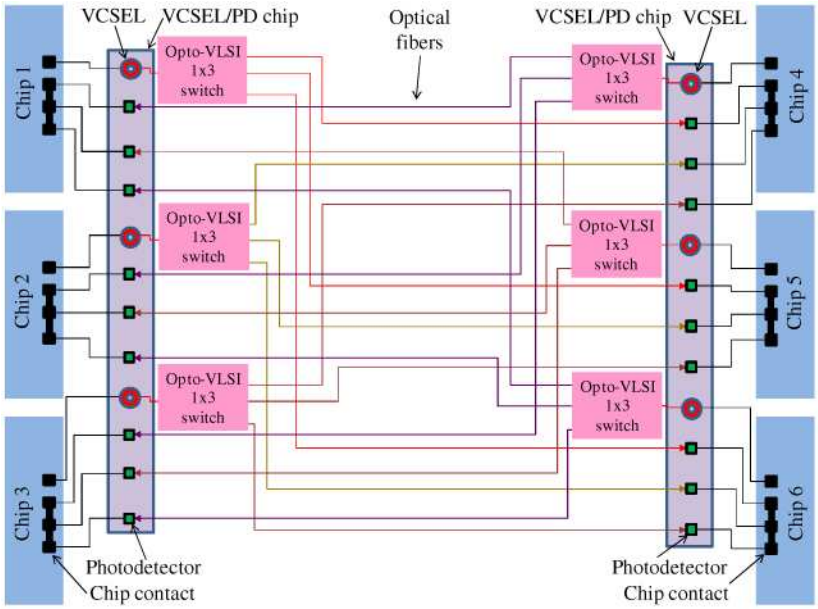

Fig. 2. Illustration of chip-to-chip reconfigurable optical interconnects employing 1x3 optical switches.

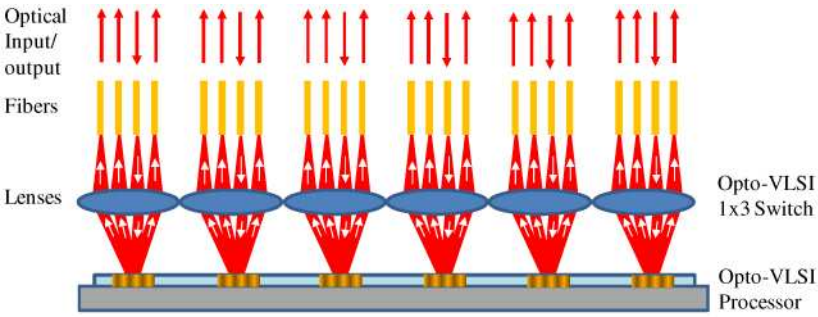

Fig. 3. Illustration of an array of 1x3 optical switches implemented using a single Opto-VLSI processor and a 4-f imaging system.

4. 4-f imaging system operation

Figure 4 illustrates the principle of the 4-f imaging system used in the optical interconnect architecture. When a blank phase hologram drives a pixel block of the Opto-VLSI processor, the optical beam diverging from the input optical fiber (fiber 2) is collimated by the 4-f imaging lens, reflected back by the Opto-VLSI processor (0^{th}-order diffraction), and then focused by the same lens onto a spot between the upper and lower optical fibers so that negligible optical power (or crosstalk) is coupled into both upper and lower fibers, as illustrated in Fig. 4(a). By driving the Opto-VLSI processor with optimized steering holograms, the input collimated beam carrying data can be steered and coupled to either optical fiber 3 or 4 ($+1^{st}$-order diffracted beams) or to optical fiber 1 (-1^{st}-order diffracted beam) as illustrated in Figs. 4(b-d). According to Eq. (1), both $+1^{st}$-order diffraction and -1^{st}-order diffraction can have their steering angles changed by resetting the phase hologram (or blazed grating) parameters.

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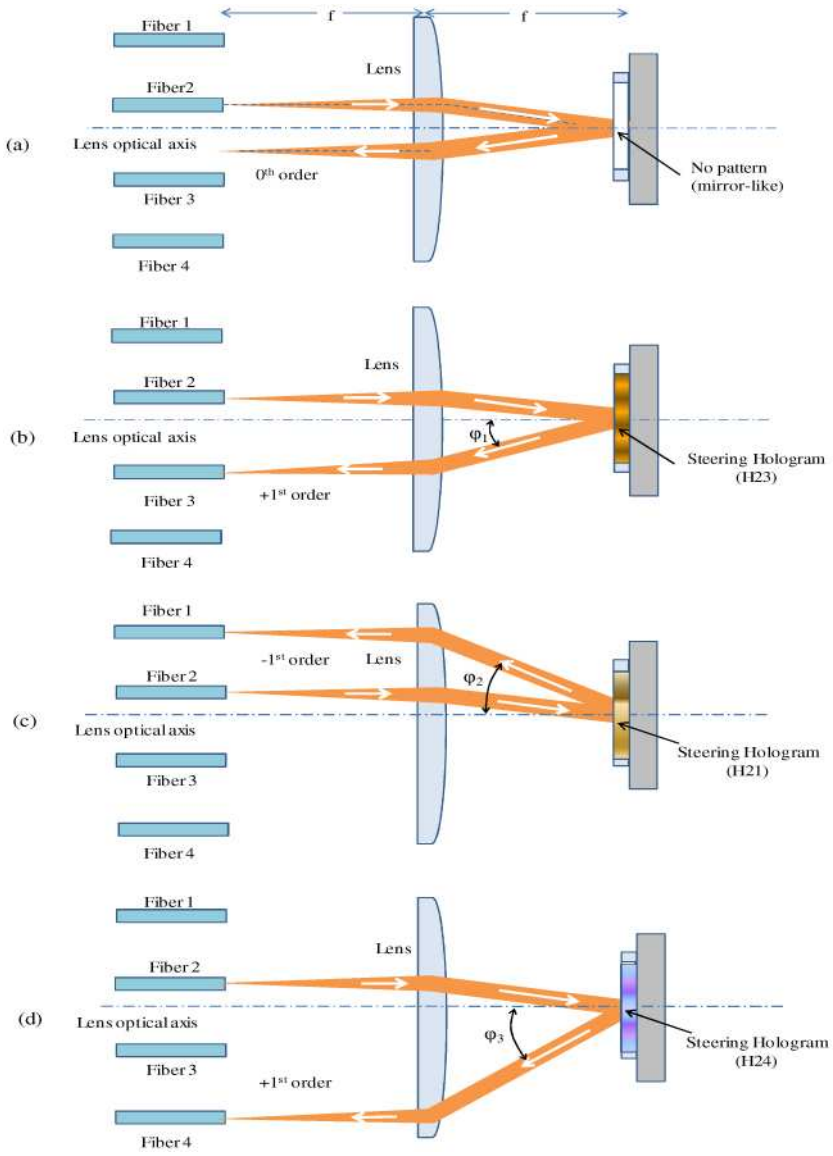

Fig. 4. Illustration of the principle of switching operations. (a) Without a hologram, the collimated optical beam reflects back and focuses on a spot between the two fibers; (b) With hologram H23 on, a $+1^{st}$ order diffracted beam is focused on and coupled into the fiber 3; (c) With hologram H21 on, a -1^{st} order diffracted beam is focused on and coupled into the fiber 1, (d) With hologram H24 on, a $+1^{st}$ order diffracted beam is focused on and coupled into the fiber 4.

5. Experiments and results

5.1 Switching operation of optical signals

In order to demonstrate the principle of the proposed optical interconnect architecture shown in Fig. 2, an experiment was set up to measure the output optical intensities from different fiber port through a 1x3 Opto-VLSI switch, as illustrated in Fig. 5. A 1-D 256-phase 4096-pixel Opto-VLSI processor was used. Each pixel has an area of 6mm×1μm with a dead space between adjacent pixels of 0.8μm. An off-the-shelf 16-port fiber array of fiber spacing 250μm was used and aligned to a lens of focal length 12.5mm. The Opto-VLSI processor was placed

#118749 - $15.00 USD Received 19 Oct 2009; revised 18 Nov 2009; accepted 19 Nov 2009; published 25 Nov 2009

at 12.5mm from the lens and aligned to form a 4-f imaging system in conjunction with the lens. Three optimized phase holograms were synthesized to steer the input optical beam of λ=1550nm from a laser source into fiber ports 1, 3 and 4 via fiber 2, respectively. Two optical spectrum analyzers (OSAs) were used to monitor the output signal intensities and crosstalk levels, respectively. In this demonstration, sufficiently large holograms were generated and uploaded into the active area of the Opto-VLSI processor for dynamic optical beam steering.

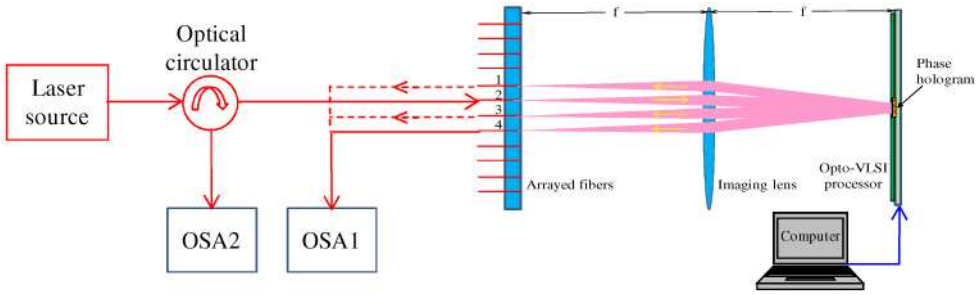

Fig. 5. Experimental system for measuring the optical intensities at the three output ports of the optical interconnect system. Optical signal from a laser source is input through fiber 2 and the three fibers are used for output ports for receiving the steered beams by the Opto-VLSI processor. Two optical spectrum analyzers OSA1 and OSA2 are used to measure optical intensities for both signal and crosstalk.

Figure 6 shows the measured optical spectra of the output signals from fiber 3 and fiber 4, which had the highest power level and lowest power level, respectively. The optical power level of fiber port 1 was between that of fiber 3 and fiber 4, as listed in Table 1. The input optical power launched to fiber 2 was +4.7dBm. Therefore, the optical switching losses were 5.8dBm for fiber 3 and 9.6dBm for fiber 4. This included fiber-to-fiber beam coupling loss, the Opto-VLSI processor loss, polarization dependent loss of around 0.6dB. The loss of fiber connectors in the system was 0.2dB. The non-uniform optical switching loss through the different output ports is mainly due to the fact that the diffraction efficiency of a steering hologram decreases with increasing the steering angle [24]. The crosstalk, defined as the ratio of the measured optical signal power at the intended fiber port and the maximum crosstalk power detected at the other fiber ports, was less than −36.4dB for all of the three output signals.

Table 1. The intensities of signals and crosstalk levels from the five fiber ports measured by OSA1 and OSA2 (Fig. 5).

Operation (Fiber port)	1	2	3	4
Power level (dBm)	–3.0	input + 4.7dBm	–1.3	–5.1
Max crosstalk power(dBm)	–41.9 (fiber2)	–49.8 (fiber3)	–42.4 (fiber2)	–41.5 (fiber2)

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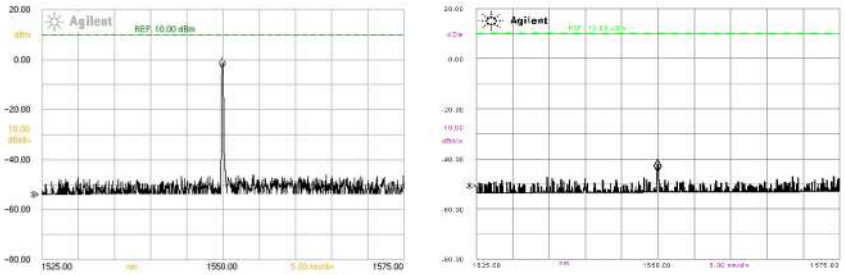
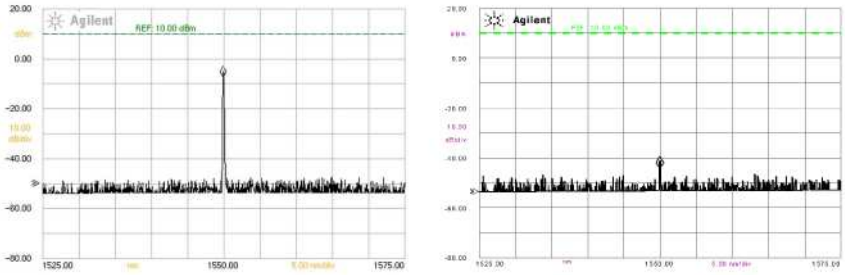


(a). Optical spectra for the signal at fiber 3 (left) and maximum crosstalk at fiber 2 (right).



(b). Optical spectra for the signal at fiber 4 (left) and maximum crosstalk at fiber 2 (right).

Fig. 6. Measured optical spectra from fiber 3 and fiber 4 and the crosstalk intensities detected by the OSA1 and OSA2.

5.2 Eye diagram measurements

Figure 7 shows the experiment that was set up to investigate the eye diagrams for data transmission through the proposed reconfigurable optical interconnects. Data synthesized by a high-speed pattern generator was used to modulate a 1550nm laser light via an electro-optic intensity modulator. A polarization controller was used to maximize the modulated optical intensity. The modulated optical signal was launched into optical fiber port 2 and switched via the 4-f imaging system to port 4. This switching scenario corresponds to the worst-case insertion loss of the Opto-VLSI-based switching operation. The switched optical signal was

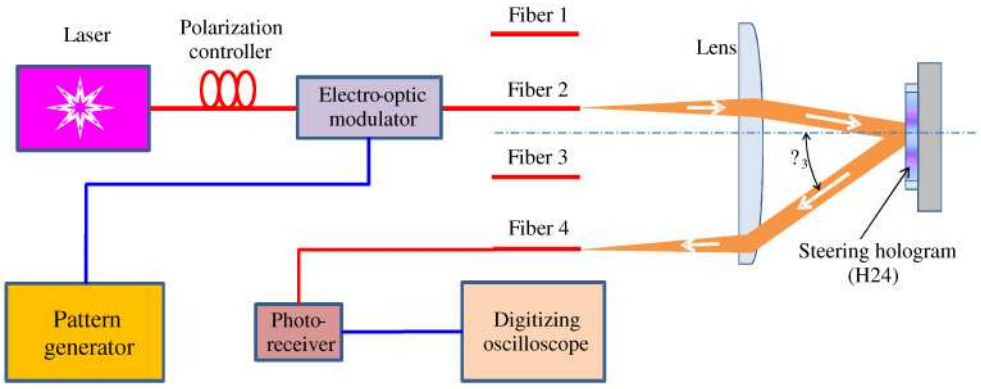


Fig. 7. Experimental setup for measuring the eye diagram of the optical interconnect architecture. Opto-VLSI processor switches modulated optical signal from Fiber 2 to Fiber 4. Insertion loss due to optical switching is around 9.6 dB (worst-case scenario).

detected by a high-speed photo-receiver and the photodetected data was monitored by a digitizing oscilloscope, where eye diagrams were displayed. Both the modulator and the photo-receiver used in the experiment have bandwidths exceeding 12GHz.

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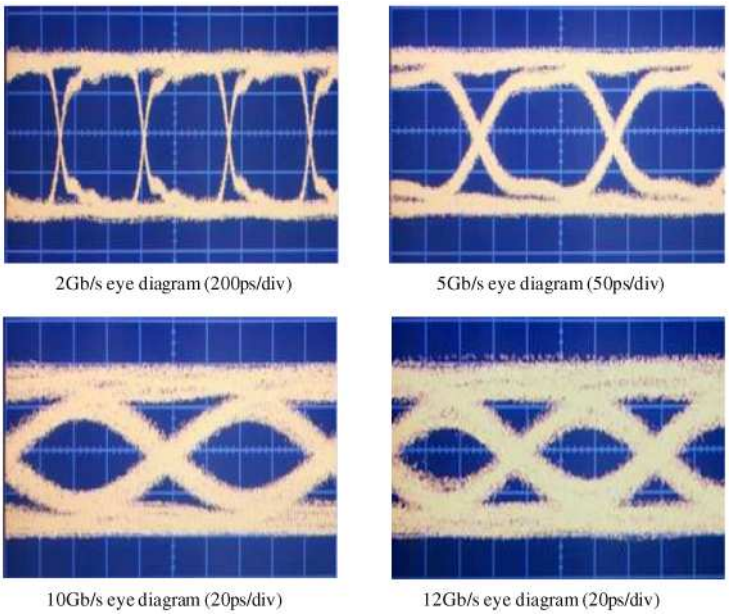

Fig. 8. Measured eye diagrams for transmitted data rate of 2Gb/s, 5Gb/s, 10Gb/s and 12Gb/s through the reconfigurable optical interconnect system.

Figure 8 shows the eye diagrams that were measured by the digitizing oscilloscope for the data rates 2Gb/s, 5Gb/s, 10Gb/s and 12Gb/s, respectively. It can be seen that the eye opening is large enough at 10Gb/s, however, it is reduced at 12Gb/s due to the reduction in signal-to-noise ratio of the transmitted data. The experiments shown in Fig. 5 and Fig. 7 and the results demonstrate the principle of the proposed reconfigurable optical interconnect architecture for high-speed chip-to-chip and board-to-board data communications.

6. Conclusion

We have presented and demonstrated experimentally a novel reconfigurable optical interconnect architecture for chip-to-chip and board-to-board high-speed data communications. The interconnect architecture employs a single Opto-VLSI processor to realize six 1x3 optical switches based on 4-f imaging. The capability of the Opto-VLSI processor to reconfigure optical interconnects has been demonstrated through the steering of modulated optical signals from an input optical fiber port to any output fiber ports by means of computer-generated holograms. Experimental results have shown that the optical switching losses range from 5.8dB to 9.6dB depending on the input-output fiber port combination, and that the crosstalk level is less than −36dB. Data transmission and eye diagram measurements have also been carried out at different bit rates, and demonstrated a large eye opening for bit rates below 10Gb/s. The proposed reconfigurable optical interconnect architecture has potential for applications in high performance computing and adaptive signal processing.

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