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***Abstract*—The design, operation, and characterization of CMOS imagers implemented using: 1) "regular" CMOS wafers with a 0.5-μm CMOS analog process; 2) "regular" CMOS wafers with a 0.35-μm CMOS analog process; and 3) silicon-on-insulator (SOI) wafers in conjunction with a 0.35-μm CMOS analog process, are discussed in this paper. The performances of the studied imagers are compared in terms of quantum efficiency, dark current, and optical bandwidth. It is found that there is strong dependence of quantum efficiency of the photodiodes on the architecture of the image sensor. The results of this paper are useful for designing and modeling CMOS/SOI image sensors.**

***Index Terms*—CMOS integrated circuits, image sensors, photodiodes, silicon-on-insulator (SOI) technology.**

I. Introduction

CMOS image sensors are currently drawing much attention because they have the potential to compete with charge-coupled device cameras. Camera-on-a-CMOS chips will be an inevitable component for future intelligent systems and are currently under intensive research worldwide because of their enormous market potential. Therefore, investigating and developing better imagers on a chip is highly important. This research focuses on new camera-on-chip architectures based on novel silicon-on-insulator (SOI) technology.

Currently, SOI technology is considered the most promising technology for improving the performance of CMOS devices without reducing dimensions. This technology offers the possibility of building electronic devices in a thin layer of silicon that is electrically isolated from the thick semiconductor substrate through the use of a buried insulating layer [1]. In the standard silicon technology, the semiconductor substrate is associated with undesirable effects, such as parasitic capacitances, high leakage currents, parasitic bipolar components, and, more importantly, interference between individual active devices or circuits built in the same integrated chip [1]–[4].

The well-known important advantages of SOI technology are the following: more effective isolation between adjacent devices implemented within SOI top (device) layer, reduced parasitic capacitances and short-channel effects, and immunization from ionization by atoms and radiations. In addition, the SOI technology provides the relative simplicity of the etching process, allowing chip back-side illumination.

The proposed new chip architecture, based on SOI and using the back-side illumination of back-side etched substrate, allows, in principle, to increase the fill factor (theoretically to 100%), to separate the photodiodes and electronics and, therefore, to eliminate the interaction between them, to implement more functions at the focal-plane pixel level and, finally, to separate the design and process optimization of photodiodes and analog readout.

This paper reports on the comparison of the performances of six CMOS image sensor architectures with front-side illumination fabricated at Tower Semiconductor Ltd. [5] using "regular" CMOS and SOI wafers, in conjunction with 0.5 and 0.35 μm processes [6].

II. Design

In general, the design of CMOS camera is based on the concept of active pixel sensors (APS) ([7]–[17] and references within). A typical block diagram of the camera is presented in [18] and [19] and includes a 2-D matrix of pixels, two addressing decoders for pixel selection during the reading phase ("Read column" and "Read row"), one decoder for reset of whole column, 1-D array of row switches and readout circuits, and analog buffers.

The matrix is organized as a square of pixels. APS can be designed on the base of n-channel MOS (nMOS) transistors, p-channel MOS (pMOS) transistors, or both nMOS and pMOS transistors (Fig. 1). Each pixel consists of one photodiode and three transistors, namely: 1) transistor M4 that performs the reset of photodiode; 2) transistor M1 that operates as a source follower; and 3) transistor M2 that operates as an analog selection switch. In addition to these elements, there are several elements, which are common within each row of APS, such as transistor M3 that provides current for the source follower and transistors M5 and M6 that operate as a pass-gate. Pixel selection is achieved by means of the row and column decoders. When activated, the selection switch connects the associated photodiode to the corresponding row bus. For the reading operation, the row decoder selects one row at a time, thereby connecting each pixel of addressed row to the matrix output. More specifically, the rows can be divided into several groups, where each group has the separate output and is served by a separate analog buffer. In this case, the row decoder selects the several rows simultaneously, one row in each group. The subsequent processing of the signal coming from the different outputs is performed by means of an analog multiplexer.

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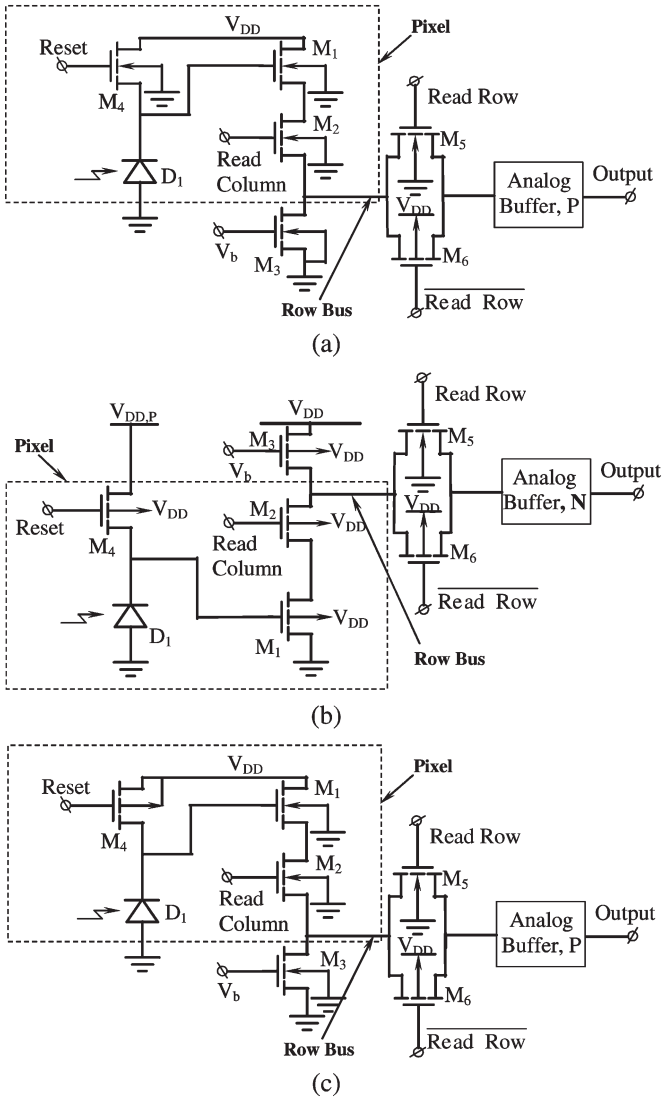

Fig. 1. Different designs of APS based on (a) nMOS transistors, (b) pMOS transistors, and (c) both nMOS and pMOS transistors.

In addition to the transistor types, APS can be designed with arbitrary dimensions, can use different types of the photodiodes, and can be fabricated using different processes. Two technologies provided by Tower Semiconductor Ltd. [5] have been attempted. The 0.5-μm technology, which is the most established "Tower's" CMOS image sensor technology, was used as a starting point of the research. The second "Tower's" technology process (0.35 μm) was run twice: for "regular" CMOS and SOI wafers, correspondingly. The "regular" CMOS wafers are p-type silicon epitaxial wafers ($\sim$16–24 $\Omega \cdot$ cm for 0.35-μm process and $\sim$24–36 $\Omega \cdot$ cm for 0.5-μm process) with epilayer thickness of $\sim$5.5-μm, whereas SOI wafers are characterized by the thickness of $\sim$675 μm, $\sim$1-μm-thick buried oxide layer and $\sim$2-μm-thick p-type top (device) layer with resistivity of $\sim$8–22 $\Omega \cdot$ cm, compatible with 0.35-μm process. The substrates SOI were supplied by CANON and prepared using the ELTRAN process [20], [21] that involves oxidized wafer bonding and water-jet separation using a predefined porous silicon layer.

The CMOS analog process 0.5 μm (twin-well on p-type epitaxial substrate, with single or double poly) of Tower Semiconductor Ltd. [5] is characterized by gate oxide of $\sim$115 Å, corresponding to the core voltage of 5.0 V, n-well/p-well depth of $\sim 1.15/1.6$ μm, correspondingly, n^+/p^+ source/drain depth of ~ 0.3 μm, and LOCOS isolation. The main highlights of the twin-well CMOS analog process (0.35 μm) (with single or double poly) of Tower Semiconductor Ltd. are listed as follows: gate oxide of ~ 70 Å, corresponding to the core voltage of 3.3 V, n-well/p-well depth of $\sim 1.2/0.9$ μm, correspondingly, n^+/p^+ source/drain depth of $\sim$0.2 μm, and using dense poly buffered LOCOS isolation. In both processes, no microlens array or color filter array had been used.

In accordance with the diode model corresponding to 0.5-μm process of Tower Semiconductor Ltd. [5], the leakage current density of n^+ imp./P-sub. diodes of large area (335×335 μm) is $\sim$0.12 μA/m^2 at room temperature. The maximum value of the leakage current density for 0.35-μm process is 1 mA/m^2 both for n^+ imp./P-sub. and n-well/P-sub. diodes at room temperature.

In this paper, the several APS implementations with the different combinations of design parameters as discussed below are compared. The total number of the imagers, which are understudy here, is six [18]. The first group of imagers is fabricated using 0.5 μm technology process within "regular" CMOS wafers and includes the matrix of 128×128 pixels ("Imager-1") and the matrix of 64×64 pixels ("Imager-2") [18]. Both "Imager-1" and "Imager-2" are based on the pixels, consisting of nMOS transistors [Fig. 1(a)] and photodiode implemented by n^+ imp./P-sub. junction, while the photodiode occupies the area, which is free from the rest of electronics. The pixel size for both imagers is 20×20 μm, while the fill factor is $\sim$35% for "Imager-1" and $\sim$47% for "Imager-2." The difference between the fill factors is due to the additional guard ring surrounding the transistors within each pixel of "Imager-1" [see pixel cross sections in Fig. 2(a) and (b)]. This guard ring is implemented by the n^+ imp./P-sub. junction, connected to $V_{\rm dd}$ and intended for elimination of the interaction between photodiodes and transistors within the pixel.

The advantage of the design with a large photodiode area is that the quantum efficiency is maximized, because the generated photocarriers have the higher probability to reach the p-n junction and to contribute to the photocurrent [22], [23]. On the other hand, a large area photodiode results in higher integration capacitance and significant leakage current, which can be the major limitation for this design.

The second group of imagers is fabricated using 0.35-μm technology process within "regular" CMOS wafers and includes a matrix of 256×256 pixels [18]. The first imager of this group ("Imager-3") is based on pixels consisting of nMOS transistors [see Fig. 1(a)], whereas the second one ("Imager-4") uses pixels based on pMOS transistors [see Fig. 1(b)]. The pixel size for both imagers is 20×20 μm, while the fill factors are $\sim$53% and $\sim$37% for "Imager-3" and "Imager-4," respectively [Fig. 2(c) and (d)]. All pixels have no guard ring. Each of the two types of APS has the photodiode implemented by n-well/P-sub. of minimal area (see Table I). The advantage of this

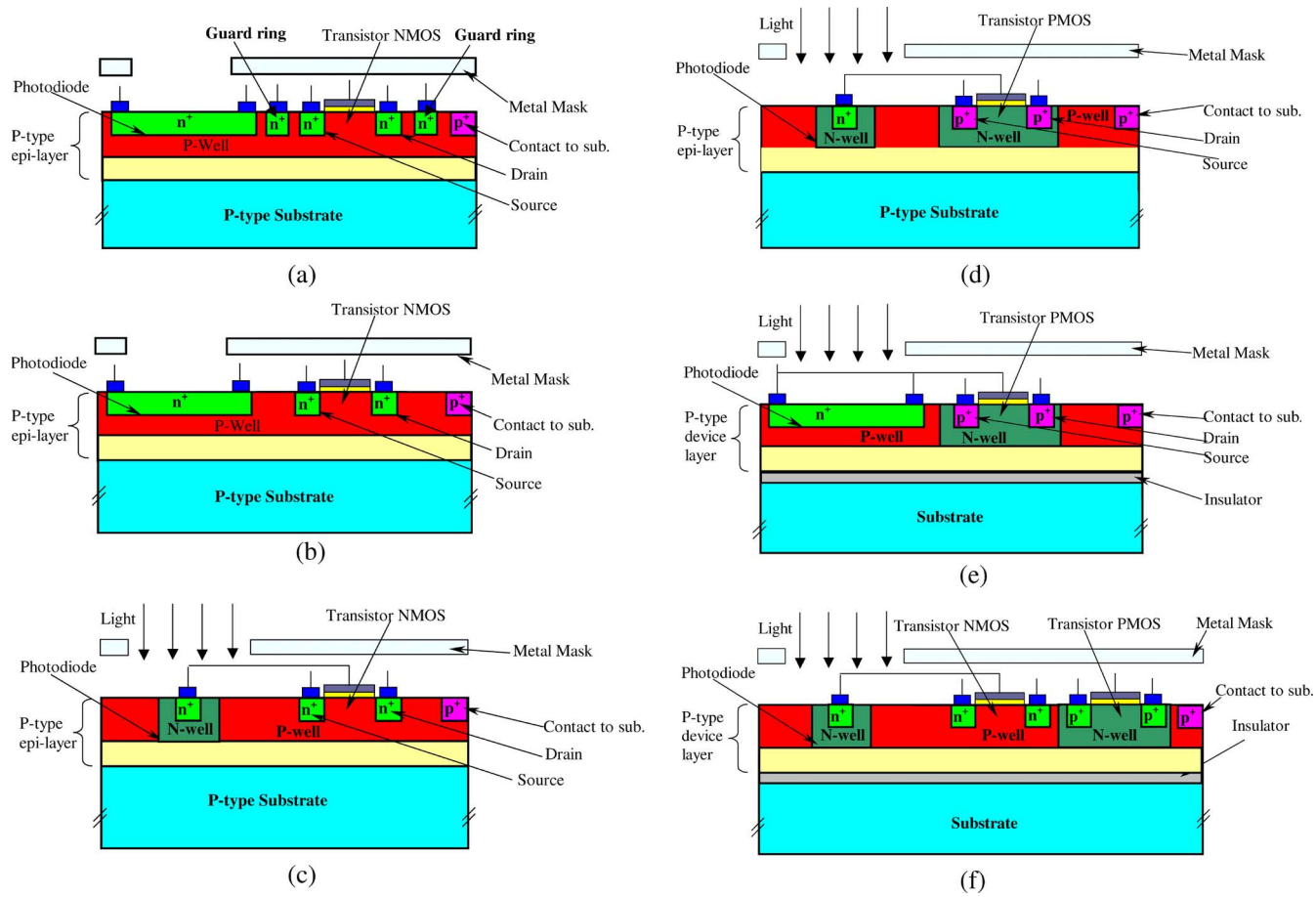

Fig. 2. Cross sections of the pixels (a–b) fabricated using 0.5-μm technology process within CMOS wafer and based on nMOS transistors with additional guard ring, (a) "Imager-1," and without guard ring, (b) "Imager-2;" (c–d) fabricated using 0.35-μm technology process within CMOS wafer and based on nMOS transistors, (c) "Imager-3," and pMOS transistors, (d) "Imager-4;" and (e–f) fabricated using 0.35-μm technology process within SOI wafer and based on pMOS transistors, (e) "Imager-5," and both nMOS transistors and pMOS transistors, (f) "Imager-6."

design is the minimal leakage current resulting from minimizing the photodiode area. On the other hand, the main disadvantage of this design is the lower quantum efficiency due to the minimal photodiode area [22], [23].

The third group of imagers is fabricated using 0.35-μm technology process within SOI wafers and also includes a matrix of 256×256 pixels [18], [19]. The first imager of this group ("Imager-5") is based on pMOS transistors [see Fig. 1(b)], whereas the second one ("Imager-6") is based on both nMOS and pMOS transistors [see Fig. 1(c)]. Both imagers have a pixel size of 10×10 μm, while the fill factor is $\sim$20% for "Imager-5" and $\sim$23% for "Imager-6." Fig. 2(e) and (f) exhibit the cross sections of these pixels. Each type of APS also has no guard ring. "Imager-5" and "Imager-6" are based on the photodiodes implemented by n^+ imp./P-sub. and n-well/P-sub. junctions, correspondingly, while each photodiode has an area close to the minimal allowed value (shown in Table I).

Thus, the different designs are classified into three groups according to the applied process and wafer type, namely: 1) 0.5-μm process in "regular" CMOS wafers; 2) 0.35-μm process in "regular" CMOS wafers; and 3) 0.35-μm process in SOI wafers. In addition, the different designs based on nMOS and pMOS transistors are compared. The main design parameters are summarized in Table I, which also specifies the structure of the designed photodiodes. Table I also summarizes measured results discussed in Section III.

III. Measurement Results

The results reported in this paper include the measurements of photodiode quantum efficiency and leakage current, and the photos are captured by the studied imagers.

The quantum efficiency was measured using a monochromator SpectraPro-150, comprising a light source, the monochromator itself, and an analog-to-digital converter. In general, the quantum efficiency is expressed as

$$\eta = \frac{hcI_\lambda}{\lambda q P_{\text{opt}} \text{FF}} \tag{1}$$

where $I_\lambda = C_d \Delta V_d / t_{\text{int}}$ is the measured photocurrent, λ is the wavelength, h is Plank's constant, c is the light velocity, q is the electron charge, P_{opt} is the total optical power, irradiating each pixel, C_d is the effective integration capacitance at the photodiode node, ΔV_d is the photodiode voltage discharging due to the light illumination, t_{int} is the integration time, and FF is the fill factor. The system was calibrated by illuminating a calibrated large-area p-i-n photodiode connected to Optical Power Meter 1830-C (New Port).

TABLE I
SUMMARY OF THE MAIN DESIGN PARAMETERS AND MEASUREMENT RESULTS

Imager type	Camera description	Process	Photo-diode type	Photo-diode area, [μm^2]	Dark current density at ~300°K, [$fA/\mu m^2$]	Peak quantum efficiency (Q.E.)	Comments
"Imager-1" (1^{-st} group)	CMOS, based on NMOS transistors, with guard ring	0.5 μm	n^+ imp. / P-type	143	0.041	~70% at ~520nm	High Q.E. and low dark current density due to the large photodiode area and process quality
"Imager-2" (1^{-st} group)	CMOS, based on NMOS transistors, without guard ring	0.5 μm	n^+ imp. / P-type	188	0.037	~70% at ~520nm	High Q.E. and low dark current density due to the large photodiode area and process quality
"Imager-3" (2^{-nd} group)	CMOS, based on NMOS transistors	0.35 μm	N-well / P-type	4	1	~40% at ~460-530 nm	Reduced Q.E. due to lower junction area (see [24])
"Imager-4" (2^{-nd} group)	CMOS, based on PMOS transistors	0.35 μm	N-well / P-type	4	0.15	~6% at ~460-520 nm	Lower Q.E. due to the large area N-well including three PMOS transistors, which competes in collecting photo-generated carriers
"Imager-5" (3^{-d} group)	SOI, based on PMOS transistors	0.35 μm	n^+ imp. / P-type	1	<<1	~2% at ~390-450 nm	Low Q.E. due to the large area N-well including three PMOS transistors, which competes in collecting photo-generated carriers
"Imager-6" (3^{-d} group)	SOI, based on both NMOS and PMOS transistors	0.35 μm	N-well / P-type	3.2	15	~40% at ~430-520 nm	The exact mechanism causing the high dark current for "Imager-6" needs to be further investigated

Fig. 3 shows the measured quantum efficiency spectra for all types of imagers. First of all, it is noticed that the quantum efficiency spectra for both "Imager-1" and "Imager-2" are very similar [Fig. 3(a)]. This proves that the additional guard ring surrounding the transistors within each pixel does not collect the photocarriers and, hence, does not prevent the transistors from diffusing the photocarriers. This phenomenon is due to the small depth of n^+ implantation region, which has insignificant interaction with photocarriers diffusing toward the transistors region. The second important observation is that both "Imager-1" and "Imager-2" exhibit a high peak quantum efficiency (∼70%) around the 520-nm wavelength and also a broad optical "bandwidth" (∼400–700 nm). These experimental results are in good agreement with previously reported structures having a relatively large thickness epilayer (∼5.5 μm) and a large photodiode area [22], [23].

Fig. 3(b) and (c) shows the measured quantum efficiency spectra for "Imager-3" and "Imager-4." It is noticed that for these imagers, the optical "bandwidth" and the wavelength at the maximum quantum efficiency are similar to those of "Imager-1" and "Imager-2." This is the result of using the same epilayer thickness for "Imager-1" to "Imager-4." On the other hand, the measured maximum quantum efficiencies for "Imager-3" and "Imager-4" (∼40% and ∼6%, correspondingly) have lower values in comparison to "Imager-1" and "Imager-2," mainly because of the smaller areas of the photodiodes of "Imager-3" and "Imager-4" [22], [23] (see Table I). The significant difference between the values of the quantum efficiency of "Imager-3" and "Imager-4" can be explained as follows. Since the pMOS transistors are implemented within n-well, each pixel of "Imager-4" has two n-wells: the first n-well forms the photodiode and the second is the n-well that includes the three pMOS transistors. The junction area of the photodiode is negligible in comparison to the area of the second n-well. Both "Imager-3" and "Imager-4" have the photodiodes of the same type and dimensions (Table I) and, therefore, the contribution of photoholes generated within n-well (as a part of the photodiode) is the same for "Imager-3" and "Imager-4." However, in "Imager-4," a substantial portion of the photoelectrons generated within the p-type epilayer contributes to the current through the second n-well, where the pMOS electronics is implemented, rather than to the photodiode current.

Fig. 3(d) and (e) displays the measured quantum efficiency for "Imager-5" and "Imager-6." First of all, one can see that the wavelengths corresponding to the maximum quantum efficiency are moved toward shorter wavelengths (in comparison to all previous imagers). The second observation is that the optical "bandwidth" is narrower both for "Imager-5" and for "Imager-6" (∼400–550 nm). These results are attributed to the lower thickness of the silicon top layer of SOI wafer in comparison with the thickness of the epilayer of CMOS wafer. As for the maximum value of the quantum efficiency, it reaches ∼40% for "Imager-6," which is similar to "Imager-3," and ∼2% for "Imager-5." The last value is very low, and

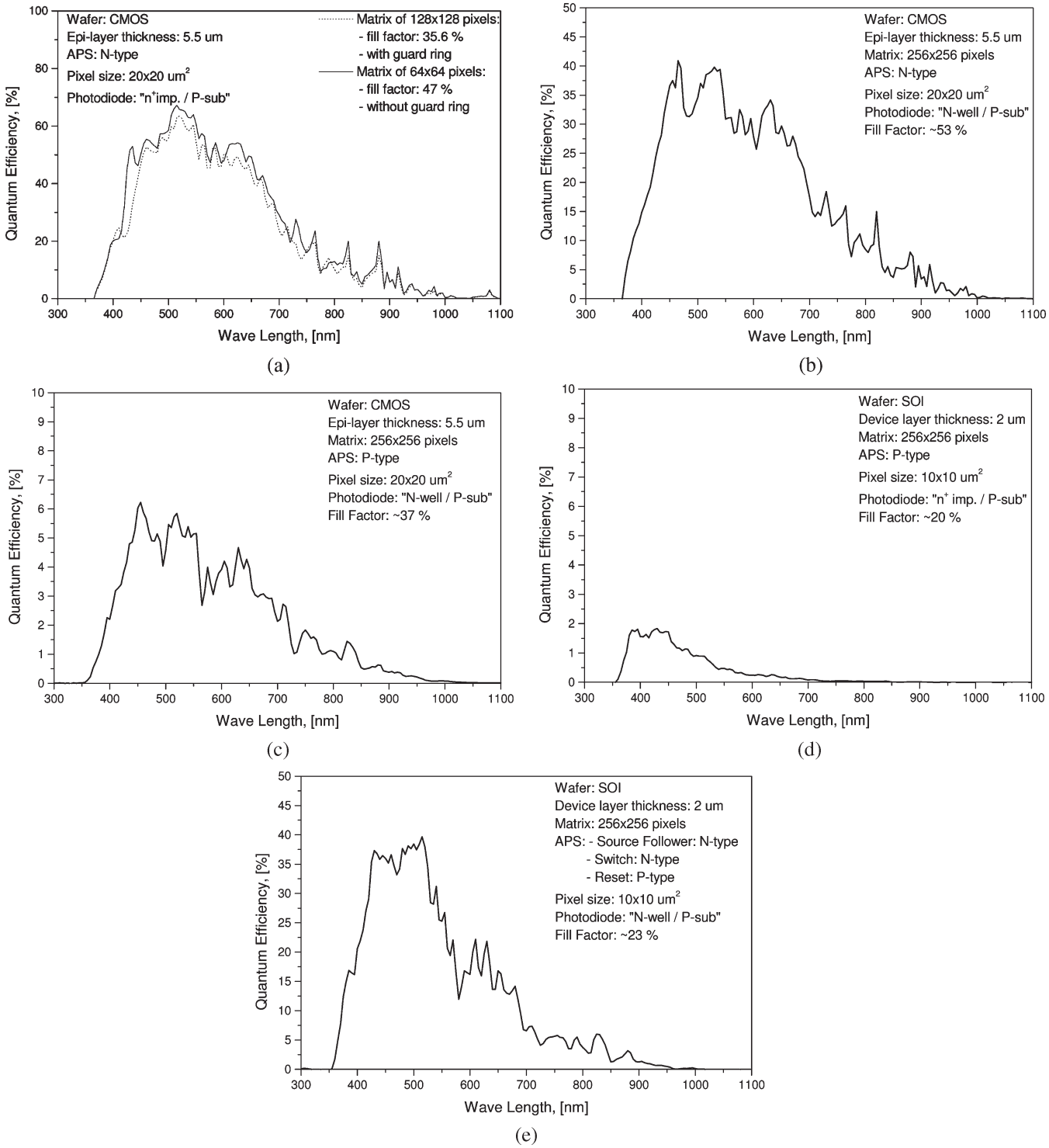

Fig. 3. Measured quantum efficiency for (a) "Imager-1" and "Imager-2," corresponding to Fig. 2(a) and (b); (b–c) "Imager-3" and "Imager-4," corresponding to Fig. 2(c) and (d); and (d–e) "Imager-5" and "Imager-6," corresponding to Fig. 2(e) and (f).

it is caused by the n-well including the pMOS transistors, which occupies most part of the pixel area. In addition, one can see that the wavelength region corresponding to the maximum quantum efficiency of "Imager-5" is shifted toward shorter wavelengths in comparison to the same parameter of "Imager-6" (Table I). The reason of this phenomenon is the n^+ implantation/p-type implementation of the photodiode in "Imager-5" [23], [24]. The relatively high quantum efficiency of "Imager-6" corresponds to that of "Imager-3," which is implemented by nMOS transistors only. This demonstrates that a relatively small-area second n-well per pixel, having a single pMOS transistor, almost has no influence on the photocarriers contribution.

Table I presents a summary of leakage (dark) current measurements [18]. For this experiment, one pixel from each matrix was chosen constantly by means of addressing

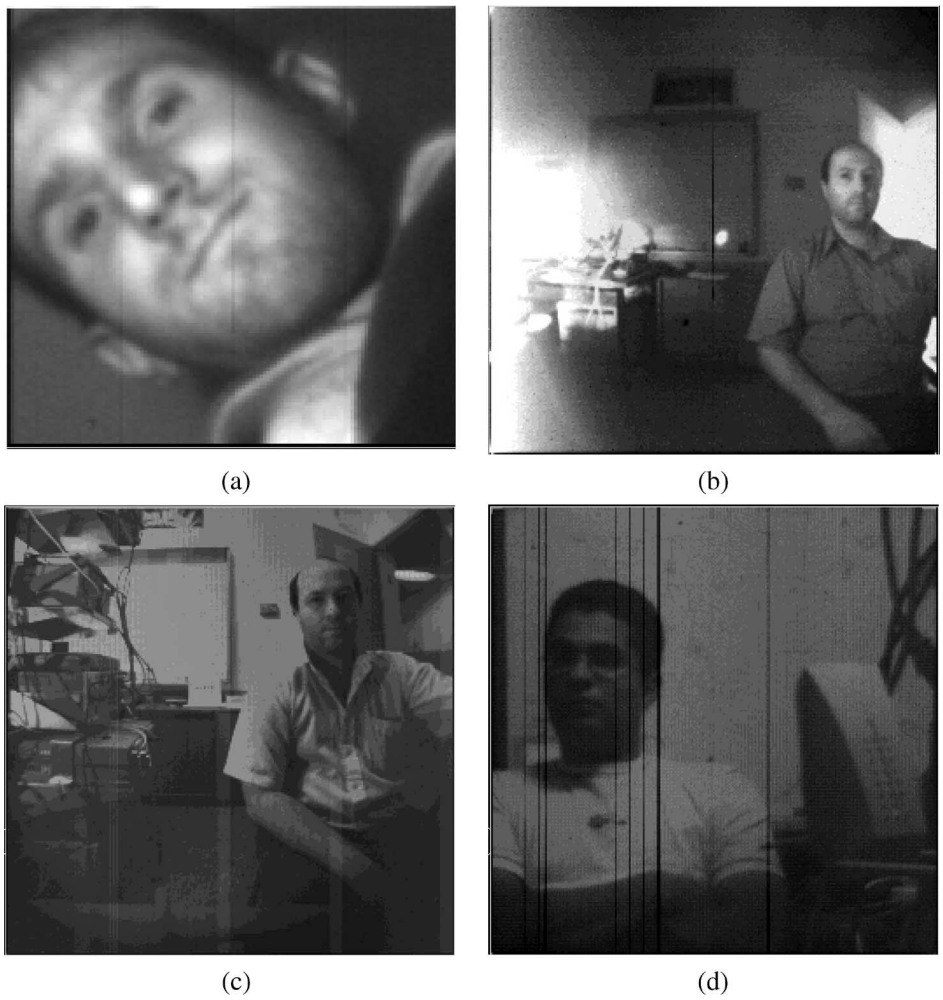

Fig. 4. Several photos that have been done by means of (a) "Imager-1," (b) "Imager-3," (c) "Imager-4," and (d) "Imager-6."

decoders, while the "Reset" transistors were connected to the low-frequency square wave with a duty cycle of 50%. When the reset signal was low, integration was performed. Knowing the integration time, voltage change, and integration capacitance at the photodiode node, it was possible to calculate the leakage current through the photodiode node. First of all, one can see that both "Imager-1" and "Imager-2" demonstrate the best results in terms of leakage current density. This was due to the large area of the photodiodes, which reduced the effect of periphery regions around the photodiode on the dark current density [22], as well as the process quality, as manifested by the reported low dark current. Second, regarding the pixel implementation (Fig. 1), the pixels based on pMOS transistors have a lower dark current density in comparison with the pixels, which are based on nMOS transistors. The reason for this result is the fact that the area of the peripheral regions contributing to the dark current was smaller for the architectures based on pMOS transistors. As explained earlier, the additional n-well required for implementing the pMOS transistor competes with the collection of the generated carriers, with the photodiodes. Thus, both the quantum efficiency as well as the dark current are reduced in this architecture, including "Imager-5" (realized using SOI wafers), which exhibits the same results as "Imager-4" based on "regular CMOS wafer. Third, the photodiodes implemented using n-well/p-type device layers fabricated within SOI wafers and referred to as "Imager-6" in Table I exhibit the highest dark current. "Imager-6" is unique in two aspects, namely: 1) it is implemented in SOI wafers and 2) it includes both nMOS and pMOS transistors. We have already demonstrated that the presence of pMOS transistors reduces the dark current. Hence, we attribute the higher dark current either to the additional interface between the p-type device layer and the buried oxide or the crystalline quality of the SOI wafers. The exact mechanism causing the high dark current for "Imager-6" needs to be further investigated.

Fig. 4 shows several photos made by the aforementioned imagers. It should be noted that the optimization of the optics was not properly done. One can see that the best quality photo corresponds to "Imager-1" (designed and fabricated using 0.5 μm process), demonstrating high quantum efficiency, wide optical "bandwidth," low leakage current density, and a relatively large number of the pixels within the matrix. This result was achieved due to the following: 1) the large area of the photodiodes; 2) the APS architecture based on only nMOS transistors, leading to the highest quantum efficiency; 3) the relatively thick epitaxial layer of the "regular" CMOS wafers

(around 5.5 μm), leading to the wider optical bandwidth; and 4) the "quality" of technology process 0.5 μm.

IV. Conclusion

This paper presents the electrooptical characterization of three groups of CMOS image sensors with front-side illumination based on the different technologies, namely: 1) CMOS 0.35 μm-technology; 2) novel CMOS/SOI 0.35 μm-technology; and 3) CMOS 0.5 μm-technology. The performances of image sensor architectures fabricated using the above technology processes have been compared in terms of quantum efficiency, dark current, and photo quality. Measured results have been compared with the quality of images captured using these image sensors with simple optics and low illumination.

It has been found that there is strong dependence of quantum efficiency of the photodiodes on the architecture of the image sensor. The maximum value of peak quantum efficiency was obtained for the architectures based on nMOS transistors, which do not contain additional n-wells. The second important factor that affected the value of quantum efficiency was the photodiode area (the larger the photodiode area, the higher the quantum efficiency). For the value of optical bandwidth, the best results were obtained for the architectures fabricated within a "regular" CMOS wafer, of epilayer thickness around 5.5 μm. SOI wafers with a device layer thickness of 2 μm exhibited a narrower optical bandwidth for all the studied imager architectures. The dark current is strongly affected by the pixel architecture, photodiode structure and dimensions, as well as the technology process. Using a state-of-the-art characterization facility, the best results were obtained for the image sensors designed and fabricated using process 0.5 μm. The measured lowest dark current correlates with transistor noise measurements, which were carried out earlier [22].

The results presented in this paper are in good agreement with [22]–[33] for CMOS APS within "regular" and SOI wafers. The single most significant feature of CMOS Image Sensors on SOI, compared to bulk, besides the shift in quantum efficiency to shorter wavelengths, is related to the leakage current. While leakage currents in various circuit designs in SOI were studied and reported [34], the specific designs reported here need to be further studied and optimized to reduce the leakage current.

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