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Guard-Ring Electrode Effects on Crosstalk in Simulated 2D CMOS Compatible Vertical Photodiode Pixel Arrays

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Abstract– In this study, we have simulated the electrical crosstalk in back-illuminated and front-illuminated photodiode arrays as a function of substrate thickness and junction depth for single junction photodiode pixels, with and without guard-ring electrodes. The physical mechanisms responsible for electrical crosstalk suppression are explained using an absorption volume proportion concept. The results obtained show that significant crosstalk suppression can be achieved for back-illuminated thin substrate guarded-pixel arrays.

Keywords-Crosstalk; CMOS; vertical photodiode; pixel array; single-junction; guard-ring electrode; simulation.

I. INTRODUCTION

Backwall-illuminated (BW) CMOS imaging arrays have a number of advantages over frontwall-illuminated (FW) arrays, including increased fill factor and the ability to tailor each pixel's colour response [1]. However, the problem of crosstalk is more significant for BW arrays. Studies to-date have concentrated on electrical crosstalk in FW arrays [2,3], although this has been extended to studies of single-junction and double junction BW arrays [4,5]. In this study, a comparative investigation of BW and FW vertical single-junction photodiode CMOS compatible arrays is presented, with attention given to explaining the effect of using guard-ring electrodes on electrical crosstalk suppression, with reference to an absorption volume proportion (AVP) statistic [5,6]. Maximum resolution means minimising electrical crosstalk and maximizing pixel central quantum efficiency (QE). Better resolution translates to smaller pixel and well pitch and ultimately to increased image resolution.

II. THEORY AND METHOD

Fig. 1 shows the reference vertical single-junction photodiode three-pixel array [5], termed the "naked-pixel" in this paper. Each pixel is defined as crystalline silicon with a p-type substrate acceptor density of $N_A = 10^{15}$ cm^{-3} and an n-type emitter donor density of $N_D = 10^{17} cm^{-3}$. The standard dimensions include pixel pitch of 50 μm, well pitch of 20 μm, well depth (junction depth or Jdepth) of 2 μm, and substrate thickness (Tdepth) of 12 μm. Each photodiode is reverse-biased at 2 volts. The incident light beam, with a wavelength of 633 nm, width of 5 μm, and total power of 0.1 μW, is scanned along the back or front surface of the array. The scanned electrical responses of the array of a particular pixel configuration are then compared for each illumination mode.

The guard-ring-electrode configuration is similar to the naked-pixel, except that each pixel's n-well has two electrodes: the inner, central image-cathode surrounded by a guard-ring-cathode, on the well, of equal bias. In 2D, the guard-ring-cathode appears as two cathodes on each side of the image-cathode [5,6].

Pixel electrical crosstalk occurs because minority carriers photo-generated in a given pixel are captured by an adjacent pixel [1,2,5]. Here electrical crosstalk is defined as any current captured by the central pixel's image-cathode for any illuminations outside the central pixel. Pixel configuration effects on electrical crosstalk are determined by calculating the quantum efficiency (QE) captured at the central pixel's central image-cathode for each beam-scan interval [5]. Simulations are performed using SEMICAD DEVICE (1994) Version 1.2, a 2D finite-element device simulator. Simulations are performed as a function of pixel well depth and substrate thickness using the naked pixel's well and substrate doping, junction biasing, electrode size and placement (Fig. 1). Optimal response resolution is defined as maximum QE at the pixel's centre with minimum response away from the pixel's centre. Maximum response inside and no response outside each pixel is the ideal response.

The AVP is used to explain the pixel's QE profile resolution. It is the proportion of incident light that is absorbed in a pixel [6]. The pixel's space charge region (SCR) AVP is proportional to the population density of drifting minority-carriers photo-generated in the SCR. The AVP for the rest of the pixel area (non-SCR AVP) is proportional to the population density of diffusing minority-carriers photo-generated in the pixel outside the SCR, in the well and in the substrate. The AVP depends on the position and extent of the SCR, the latter being determined by the doping, biasing and geometry of the pixel's structural components. As such, the AVP represent a basis for understanding the extent to which the pixel's response resolution is dependent on the location of photo-generation of minority carriers and the location and extent of the SCR.

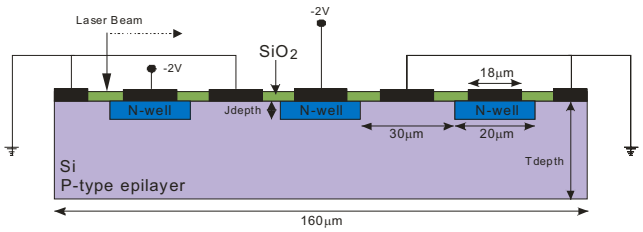

Figure 1. Cross-section of the simulated frontwall-illuminated photodiode array. The backwall-illumination mode involves the laser illuminating the underside of the array.

III. RESULTS

Fig. 2 and Fig. 3 show the response of BW and FW pixels against laser position, for both naked and guarded pixel configurations. Shown are "substrate thickness/well depth" combinations of the "12µm/4µm" (Fig. 2) and "3µm/1µm" (Fig. 3) pixels. The graphs show combinations of the total-QE and electron-QE (nQE) that are associated with the central pixel's central image-cathode (x = 80µm) as well as the total-QE and nQE associated with the central pixel's left guard (L-guard) cathode (at x = 55µm) for the guarded pixel case. QE responses are shown for an illumination position window between the left boundary of the central pixel (x = 55µm) and the centre of the central pixel (x = 80µm). The left half of the central pixel's well extends from laser position x = 70µm to position x = 80µm. The chosen well depth for each figure has the best sensitivity and crosstalk suppression for the two substrate thicknesses considered.

Fig. 4 shows the response of BW and FW pixels against substrate thickness, for both naked and guarded pixel configurations of 1µm well depth. Fig. 5 is the corresponding AVP profiles for the pixel configurations considered in Fig. 4. Fig. 6 show the response of BW and FW pixels against well depths, for both naked and guarded pixel configurations of 12µm substrate thickness. Fig. 7 is the corresponding AVP profiles for the pixel configurations considered in Fig. 6.

Figs. 2 and 3 indicate the guard-cathode capturing the electrical crosstalk that is also captured by the naked image-cathode. This is indicated by the parallel QE response of the guard-cathode to the naked image-cathode response from the pixel boundary up to the pixel well. For illuminations over the well, the guard-cathode response reduces, while the guarded-pixel's image-cathode response is increased. This is due to the guard-cathode's and image-cathode's field competing for the photo-carrier capture volume across the pixel; the guard field dominating away from the pixel's centre while the image field dominating towards the pixel centre.

The greater the proximity of the SCR to the point of illumination the greater is its capture of photo-carriers, indicated by an increase in SCR AVP and QE response of the capturing electrode. Thus the BW guard-cathode QE parallels (Fig. 2 to 3) the decreasing SCR AVP profile as the substrate thickens for illuminations over the well wall (x = 70µm) and at the pixel centre (x = 80µm) (Fig. 5). There is no change in SCR AVP for the FW pixel of constant well depth as the substrate thickens (Fig. 5) as there is no change in proximity of the SCR to the point of illumination. The slight increase in the FW pixel central QE (Fig. 4) is due to the increase in non-SCR AVP (Fig. 5), indicating a greater population of diffusing carriers contributing to the image-cathode's capture volume.

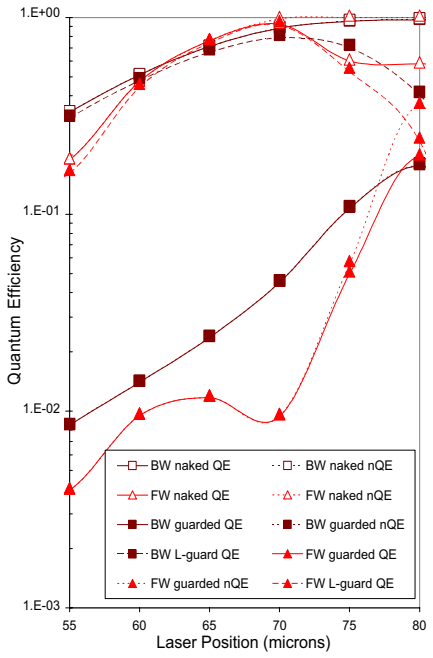

Figure 2. Quantum efficiency of BW and FW guarded and naked SJPD pixels of 4 µm junction depth and 12 µm thickness against laser position.

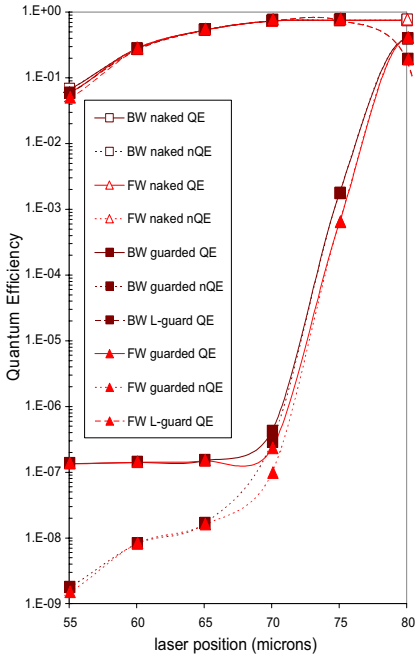

Figure 3. Quantum efficiency of BW and FW guarded and naked SJPD pixels of 1 µm junction depth and 3 µm thickness against laser position.

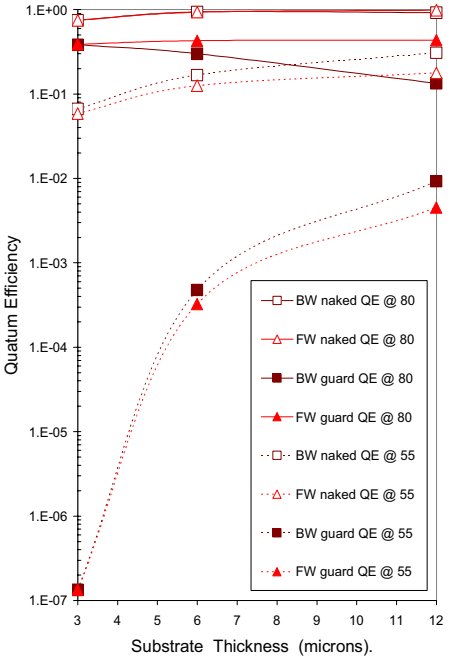

Figure 4. Quantum efficiency of BW and FW guarded and naked SJPD pixels of 1 µm well depth against thickness for the pixel's central and boundary illumination.

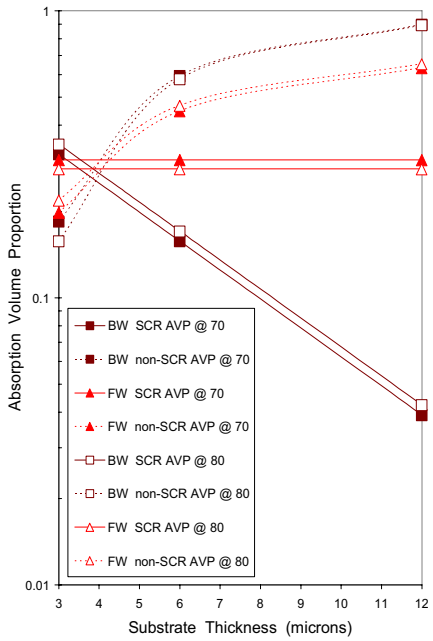

Figure 5. SCR-AVP and non-SCR-AVP of BW and FW pixel of 1 μm well depth against thickness for the pixel's central and boundary illumination.

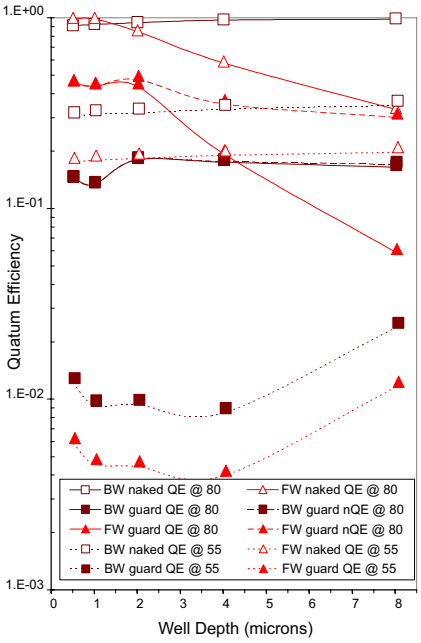

Figure 6. Quantum efficiency of BW and FW guarded and naked pixels of 12μm thickness against well depth for the pixel's central and boundary illumination.

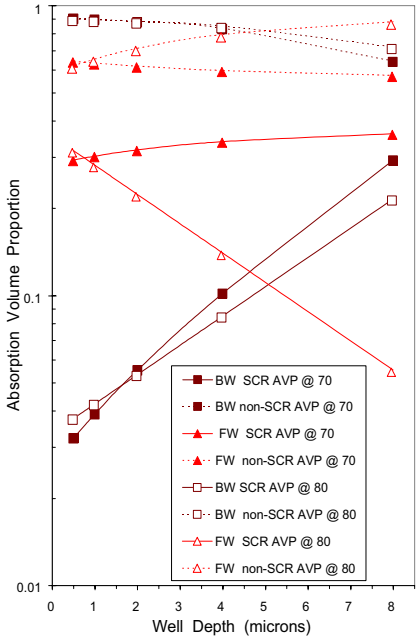

Figure 7. SCR-AVP and non-SCR-AVP of BW and FW pixel of 12 μm thickness against well depth for the pixel's central and boundary illumination.

Both FW and BW pixels are benefited similarly for the thinnest pixel. This is because the proximity of the SCR to the point of illumination becomes equally proximate for both illumination modes as the substrate thins (Fig. 2 to Fig. 3, and Fig. 4) and so their QE responses converge. This benefit to the QE response resolution and crosstalk suppression is associated with a maximum SCR AVP and a minimum non-SCR AVP for both naked and guarded pixels (compare Fig. 4 with Fig. 5). The best configuration maximizes drifting-carrier capture volume and minimizes capture volume for diffusing carriers. This benefit to the guarded pixel is due to the BW guard-cathode's capture volume being benefited by an increasing SCR AVP while BW and FW guard capture volume are benefited by a decreasing non-SCR AVP (Fig. 5) as the substrate thins from Fig. 2 to Fig. 3.

The advantages of the guarded pixel over the naked pixel can be seen not only in crosstalk suppression, but also the suppression of the effect of negative minority hole-current photo-generated increasingly in the well, for increasing well depth. However, for the thickest substrate (Fig. 2), even though central QE (sensitivity) suppression, associated with the hole current, is reduced, the proportion of the hole-QE to the total-QE has not significantly changed from that of the naked pixel. The proportion of hole-QE to total-QE decreases from the thickest to thinnest pixel (Fig. 2 to 3) because less hole current is photo-generated in pixels with shallower wells. Furthermore the BW pixel configurations have less light absorbed in the well compared to the FW mode and thus demonstrate less of a hole problem. In the 3/1 pixel (Fig. 3), the hole problem is suppressed the most, with the relative proportion of hole-QE to total-QE being reduced 4.4 fold and 34 fold for the FW and BW pixels, respectively. The hole concentration is dependent on the well depth as well as the proximity of the incidence of illumination to the well. The quantum budget expended in the well for the FW mode is greater than the BW mode as illumination is incident on the well surface.

Compared to the naked pixel the sensitivity reduction is two fold for BW and FW 3/1 guarded pixels (Fig. 3) which have the best crosstalk and sensitivity [5, 6]; the naked BW and FW 3/1 pixel QE is 75%. The guarded 3/1 is still twice as sensitive as the guarded 12/4 and with such crosstalk suppression, a four fold physical pixel resolution increase is achievable, with well pitch unchanged. This is for the SJPD pixel's (Fig. 1) doping, biasing and optimum guard ring width (6.4μm) and position (1μm from well edge) and image-cathode width of 0.4μm [6].

The BW pixel's central SCR AVP (which is a measure of the drift component of the current) increases with well depth increase (Fig. 7), while the inverse is true for central non-SCR AVP (which is a measure of the diffusion current component). The FW pixel's central AVP profiles are reversed. The BW and FW central QE responses (Fig. 6), for both naked- and guarded-pixels follow their associated SCR AVP trend. This is due to the BW pixel's increasing proximity to the bottom edge of the SCR for increasing well depth, and the reverse being true

for the FW pixel. The BW guarded pixel's central response tends to plateau due to the guard capture field increasing in tandem and competing with the image capture field, a phenomenon not present in the naked pixel.

IV. Discussion

The results show that there is a dynamic competition between the guard and image electrodes for carrier capture volume. By varying the pixel configuration, it is possible to tailor a response so that the image electrode dominates for illuminations toward the pixel centre while the guard-ring cathode dominates for illuminations away from the pixel centre. This is influenced by the proximity of the SCR to the point of illumination as well as the SCR volume, both being measured by the AVP statistic and both controlled by the pixel geometry, doping and biasing.

Generally, the FW arrays have better response resolution and crosstalk reduction than the same BW array, due primarily to their greater SCR AVP, resulting from the closer proximity of their photogenerated carrier volume to the SCR. However, as the FW and BW pixel AVPs converge, their response resolution becomes less distinguishable.

For both BW and FW pixels, the guarded pixel showed considerably less crosstalk than the naked pixel. The guard electrode captures the majority of image carriers away from the pixel centre, following what would be the naked pixel's response profile, as the guard ring and image electrode compete for the total image capture volume. The wider the guard electrode, the greater the pixel's response resolution and the less the crosstalk. However, for thicker substrates, crosstalk carriers can diffuse under the guard capture field, reducing the response resolution.

Guard pixel sensitivity (maximum QE) is inferior to that of the naked pixel because the guard-cathode capture volume dominates for the electrode sizes considered. A trade-off between crosstalk and sensitivity may be realized by adjusting the cathode sizes and pixel thickness that may result in sensitivity levels similar to that of naked pixels, while maintaining significant crosstalk reduction.

The advantage of the thinner substrate guarded pixel is that the photo-generated image carrier volume can be immediately presented to the image pixels depletion region, with appropriate mix of bias and doping, with only a shallow well. This maximizes image carrier drift that benefits image frame capture speed for fast turn around imaging applications.

V. Conclusions

In this paper, we have examined the effects of various pixel structures on electrical crosstalk in FW and BW guard-ring CMOS vertical single junction photodiode arrays. Generally, the FW arrays have better crosstalk reduction than the same pixel-configuration BW arrays, due mainly to the relative location of photo-carrier generation to the pixel's depletion region. Irrespective of illumination mode, the guarded pixel showed considerably less crosstalk than the single junction conventional pixel, due to the guard-ring electric field that forms a curtain around the central image electrode field. The guarded pixel shows a marked improvement over the conventional pixel, especially for the thinner substrates (3μm).

Optimal response resolution in guarded pixels may be predicted by the SCR AVP being maximum and greater than the pixel's non-SCR AVP, while the pixel's substrate and well AVPs are minimized, indicating less carriers diffusing under the guard-ring capture field and less negative minority current in the well, respectively. Though the predictive value of the AVP data for optimal pixel response resolution is evident, simulation is still the necessary final arbiter without the more costly fabricated-device testing option available. The AVP data can present a selection of possible optimals from which simulation can determine the most optimal pixel configuration. This AVP data here suggests that the most optimal pixel has a shallow well and a substrate depleted as fully as is practical for its application.

Overall, the results indicate the prospect of obtaining significant crosstalk suppression in BW CMOS imaging arrays through achievable modifications to the array and electrode configuration. The extent to which AVP statistics can be used for predicting pixel configurations having optimal electrical response resolution and optimal sensitivity requires further investigation; some progress already being made [6].

Acknowledgment

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References

[1] S. Hinckley, E.A. Gluszak, & K. Eshraghian, "Modeling of device structure effects in backside illuminated CMOS compatible photodiodes". Proceedings of COMMAD 2000, Melbourne. IEEE Press, 2002, pp. 399 – 402.

[2] I. Brouk, Y. Nemirovsky, S. Lachowicz, E.A. Gluszak, S. Hinckley, & K. Eshraghian, "Characterisation of crosstalk between CMOS photodiodes", Solid State Electronics, 46, 2003, pp. 53-56.

[3] J. Briaire, & K.S. Krisch, "Principles of substrate crosstalk generation in CMOS circuits", IEEE Transactions on Computer-Aided Design Of Integrated Circuits And Systems, 19(6), 2000, pp. 645 – 653.

[4] S. Hinckley, P.V. Jansz, E.A. Gluszak,, & K. Eshraghian, "Modeling of device structure effects on electrical crosstalk in back illuminated CMOS compatible photodiodes". Proceedings of COMMAD 2002, Sydney. IEEE Press, 2002, pp. 397 – 400.

[5] S. Hinckley, P.V. Jansz-Drávetzky & K. Eshraghian, "Pixel structural effects on crosstalk in backwall illuminated CMOS compatible photodiode arrays". Proceedings of DELTA 2004. 28-30 January, 2004. Perth,, Western Australia.. Los Alamitos, California: IEEE Computer Society. 2004, pp. 53 – 58.

[6] P.V. Jansz-Drávetzky, "Device structural effects on electrical crosstalk in backwall illuminated CMOS compatible photodiode arrays". B.Sc. (Physical Science) Honours Thesis. Edith Cowan University. Perth, Western Australia 2003.