2005

A Digital Pixel Sensor Array With Programmable Dynamic Range

Alistair Kitchen
Edith Cowan University

Amine Bermak
Hong Kong University of Science and Technology

Abdesselam Bouzerdoum
University of Wollongong

10.1109/TED.2005.859698
Kitchen, A. , Bermak, A., & Bouzerdoum, A. (2005). A Digital Pixel Sensor Array With Programmable Dynamic Range. Transactions on Electron Devices, 52(12), 2591-2601. Available here

A Digital Pixel Sensor Array With Programmable Dynamic Range

Alistair Kitchen, *Student Member, IEEE*, Amine Bermak, *Senior Member, IEEE*, and Abdesselam Bouzerdoum, *Senior Member, IEEE*

***Abstract*—This paper presents a digital pixel sensor (DPS) array employing a time domain analogue-to-digital conversion (ADC) technique featuring adaptive dynamic range and programmable pixel response. The digital pixel comprises a photodiode, a voltage comparator, and an 8-bit static memory. The conversion characteristics of the ADC are determined by an array-based digital control circuit, which linearizes the pixel response, and sets the conversion range. The ADC response is adapted to different lighting conditions by setting a single clock frequency. Dynamic range compression was also experimentally demonstrated. This clearly shows the potential of the proposed technique in overcoming the limited dynamic range typically imposed by the number of bits in a DPS. A 64 $\times$ 64 pixel array prototype was manufactured in a 0.35-μm, five-metal, single poly, CMOS process. Measurement results indicate a 100 dB dynamic range, a 41-s mean dark time and an average current of 1.6 μA per DPS.**

***Index Terms*—CMOS imager, digital pixel sensor (DPS), self-resetting asynchronous pixel.**

I. Introduction

CHARGE-COUPLED DEVICE (CCD) imagers remain in the forefront of commercial imaging technology, exploiting advanced manufacturing techniques to produce high quality, high resolution images. However, recent developments in CMOS image sensors have demonstrated the inherent advantages of this technology, which are particularly attractive for combined on-chip image acquisition and processing, featuring low power and low manufacturing cost [1]. Technology scaling has played a key role in introducing more intelligence and further processing even at the pixel level. A digital pixel sensor (DPS), which performs the analog-to-digital conversion (ADC) at the pixel level, is an example of the new design concepts made possible due to the scaling of CMOS devices to deep submicrometer levels. Wandell *et al.* have argued the importance of multiple image capture, and the application of DPS arrays, stressing the value of "local memory" within the imager [2]. In addition, very low-speed converters can be used and a high level of parallelism is obtained using ADCs operating at only tens of samples per second [3], [4]. An efficient exploitation of the parallelism can reduce global power consumption and speed-up data conversion, thus increasing the frame rate of the imager [3], [5]. Additional benefits are also found in DPSs as driving a large data bus using small on-pixel buffers is avoided by the use of local on-pixel data-converters. While on-pixel data conversion provides a number of advantages, there are still many challenges and issues that remain to be solved. Indeed, since the conversion in a DPS architecture takes place at the pixel level, the dynamic range is limited by the number of bits used for the conversion. Adaptation to different lighting conditions and extended dynamic range required for natural lighting scenes is very critical when designing DPS arrays.

One interesting way to improve the dynamic range of CMOS imagers is to employ time-based conversion using self-resetting architectures based on either pulse frequency modulation (PFM) scheme [6]–[10] or pulse width modulation (PWM) scheme [11]–[13]. The self-resetting scheme improves the dynamic range by recycling the well such that higher photocurrents are detected. The output takes the form of a series of spikes, resulting in the so-called "spiking pixel' [7], which is of particular interest when mimicking the processes of biological vision [9]. This method presents several issues when dealing with high resolution pixel array. One issue is related to the access to the spiking pixel array which is provided by a complex bus-arbitration system termed address event representation (AER). Another problem encountered in the AER-based imagers is the temporal jitter due to the collision problem which affects the SNR. In addition, the synchronous self-resetting scheme suffers from higher dynamic power consumption as the pixel is constantly allowed to fire whenever it reaches a threshold voltage. Therefore, the power consumption of a large array of free running pixels can be very significant. Furthermore, DPS is very inefficiently realized using the synchronous self-resetting scheme as an area consuming digital counter is required at the pixel level [6].

In this paper, a DPS array with a time-based ADC is presented. This proof-of-concept design is intended as an evaluation testbed, to assess the suitability of the device for image capture, and develop low level image processing algorithms which exploit the advantages of the DPS architecture. The pixel relies on a single pulse (or pulsewidth modulation) as well as a novel self-resetting approach using a pixel level SR latch. The pulsewidth modulation (PWM) encoding reduces the dynamic power consumption and preserves the advantage of wider dynamic range as each pixel sets its own integration time which

Manuscript received May 3, 2005; revised September 6, 2005. This work was supported in part by the Australian Research Council. The review of this paper was arranged by Editor J. Hynecek.

A. Kitchen is with the School of Engineering and Mathematics, Edith Cowan University, Joondalup 6027, Australia (e-mail: a.kitchen@ecu.edu.au).

A. Bermak is with the Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Kowloon, Hong Kong (e-mail: eebermak@ust.hk).

A. Bouzerdoum is with the School of Electrical, Computer and Telecommunications Engineering, University of Wollongong, Wollongong, NSW 2522, Australia (e-mail: a.bouzerdoum@ieee.org).

Digital Object Identifier 10.1109/TED.2005.859698

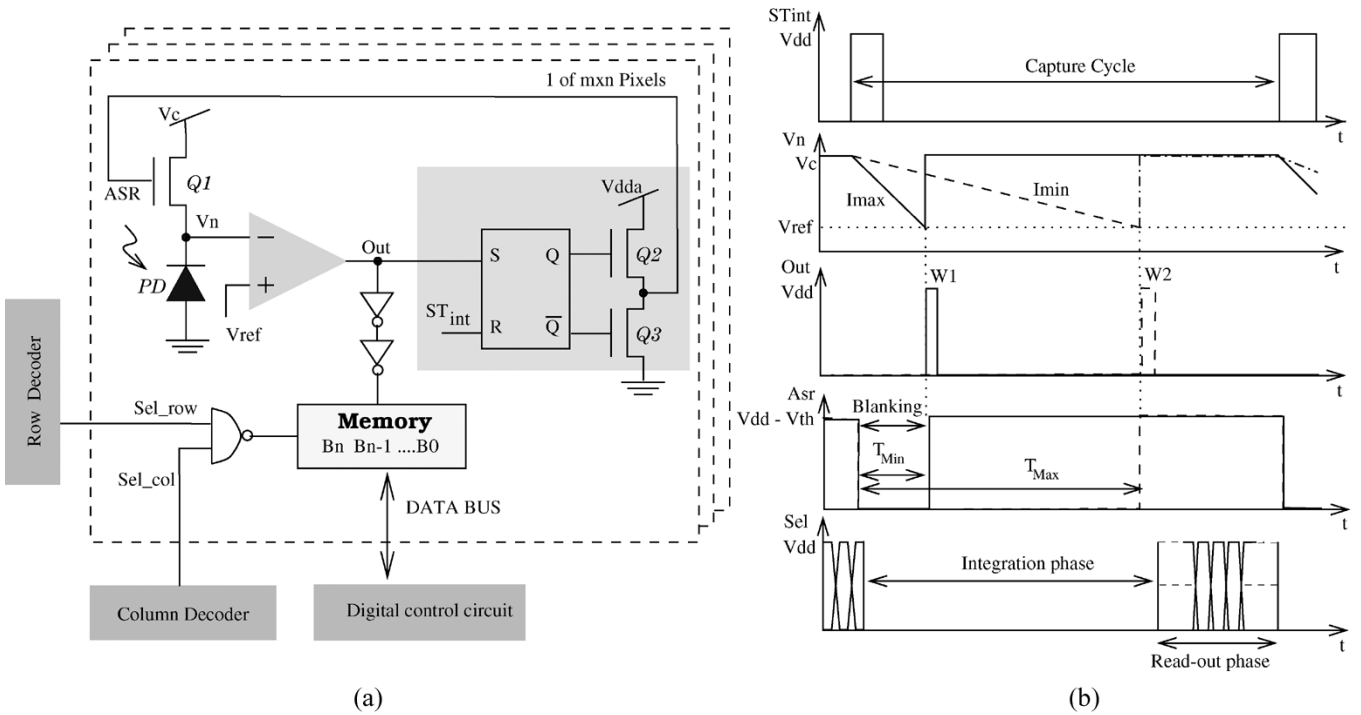


Fig. 1. (a) Architecture of the DPS array based on the self-resetting asynchronous pixel. (b) Timing diagram.

is not dictated by a global timing circuit. The sensor also integrates a pixel level memory, avoiding the need for AER type of read-out and providing focal-plane image storage capability. The conversion characteristics of the DPS are set using an array-based control circuit which in fact provides the quantization boundaries for the time domain conversion. One unique feature of our sensor is the possibility to program these quantization boundaries, effectively allowing the sensor response to adapt to different lighting conditions. Linear and extended-range non linear responses are experimentally demonstrated.

The remainder of this paper is organized as follows. Section II describes the imager architecture, including a detailed description of the self-resetting pixel operation. The time domain ADC is described in Section III, which includes simulation results of the conversion process. Section IV details the very large-scale integration (VLSI) implementation of the control circuit and the pixel. Section V presents experimental results obtained from the manufactured prototype. Section VI concludes the paper.

II. DPS With Self-Resetting Asynchronous Scheme

Fig. 1(a) and (b) shows the architecture of the self-resetting asynchronous DPS and its timing diagram, respectively. The architecture is similar in configuration to a single slope ADC, and also to the DPS array of Kleinfelder *et al.* [5]. However, our DPS array differs significantly from the other two architectures in its mode of operation. The image acquisition starts by sending a global start integration signal $\mathrm{ST_{int}}$, to the array and to the control circuit. The control circuit generates timing data, which is distributed in parallel to all the pixels of the array. Upon receiving the start integration signal, each pixel operates asynchronously, where the output voltage of the photodiode is compared to a fixed reference voltage. When the two voltages become equal, the comparator switches, and the data value, which records the switching time, is stored in the pixel memory. The integration time is therefore not dictated by a global timing circuit but is set by each pixel independently. Due to the asynchronous nature of the pixel operation, it is necessary to distribute the timing data as Gray code, to eliminate any errors that may have been caused by the pixel comparator switching during data transition. A secondary benefit of distributing the data in Gray code is reduced power consumption, as only one bit changes state per clock cycle, and only one bus line has to be charged or discharged. The photodetector operates in photon flux integration mode, where the photocurrent is integrated over time in order to produce a large change in the stored charge, and consequently, the signal voltage. This mode of operation is commonly used by most CMOS voltage mode photodetectors, and results in the junction voltage decaying at a virtually constant rate, despite the junction capacitance being voltage dependent [14]. The photodiode sensor is reverse-biased by a fixed voltage source V_C, which fully charges the photodiode junction capacitance C_J. V_C is then removed, and the junction capacitance is now discharged by the leakage current of the diode, comprised of thermally and optically generated carriers. In other sensor designs, this discharge takes place for some fixed time period, after which V_n is read and digitized, either at the array, column, or pixel level. The alternative technique presented here allows C_J to discharge to a fixed voltage reference, V_{Ref}. The time taken for this transition is measured, and the result is stored in pixel memory. The operation of the pixel, shown in Fig. 1(a), begins in the idle state, with the node V_n held at V_C by Q_1, which in turn is held ON by the SR latch, Q_2 and Q_3. V_C must be at least $2V_{\mathrm{th}}$ below V_{dda}, where V_{th} is the n-type FET threshold voltage. If this were not the case, variations in V_{th}, which is heavily process dependent, would be reflected as fixed pattern noise (FPN) in the captured

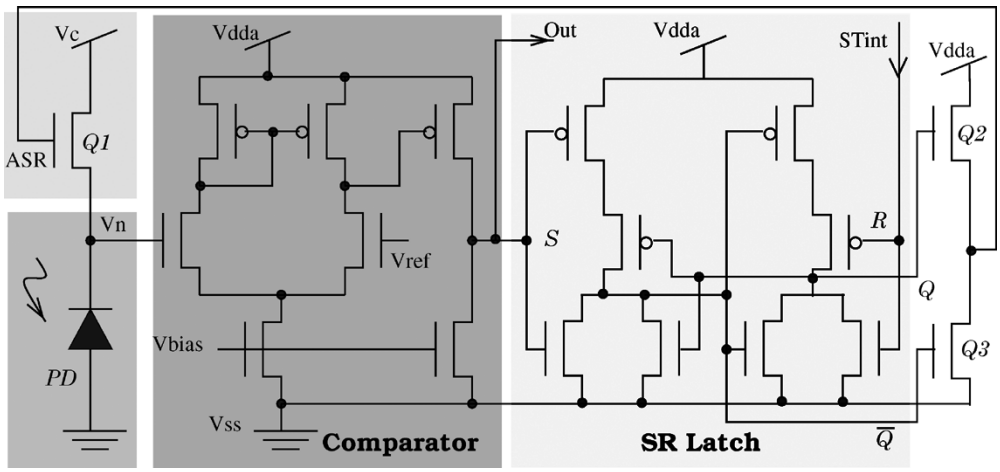


Fig. 2. Transistor level circuit diagram.

image. To begin the integration period, the signal $\mathrm{ST_{int}}$ is applied to the R input of the latch, switching the output states and turning off Q_1 (via Q_2 and Q_3). With transistor Q_1 now open, the junction capacitance is discharged by the photocurrent until $V_n = V_{\mathrm{Ref}}$. At this point the comparator output switches high, and the latch again changes state, rapidly recharging C_J, and returning the circuit to the idle state. This ensures that V_n never reaches a level where the photodiode may be forward biased, hence avoiding "blooming" of the image. This also minimizes the recharging current required for the subsequent image capture, as C_J is never fully discharged. Fig. 2 shows the transistor level circuit diagram of each pixel comprised of a photodiode sensor, an analogue comparator, an SR latch, and an 8-bit memory cell. The two-stage comparator includes a differential first stage followed by a biased-inverter.

An analogue, rather than a clocked, comparator was chosen to minimize the switching noise and to remove the need for multiphase clock distribution throughout the pixel array. Due to the self resetting circuit, the maximum comparator output voltage is typically 1.8 V, and must first be buffered to ensure reliable operation of the memory. The transistors in the first inverter stage are sized to lower the input threshold voltage to approximately 1.2 to 1.3 V, which provides an acceptable noise margin. The comparator output splits into two paths: the first controlling the self-resetting operation, and the second enabling the memory for writing. Following the comparator is an SR latch, which controls the self-resetting operation. Unlike in the PFM pixel, this does not result in a free-running multivibrator, but instead the pixel is held in a "ready" state at the end of each capture. The capture cycle is defined by two distinct phases, namely the integration and the read-out phases. During the integration phase the charges are collected during a pixels self-defined integration time. During the read-out phase, the row and column decoders are used to scan the contents of the in-pixel memories. The Q and $\overline{Q}$ outputs of the SR latch are buffered by Q_2 and Q_3, and are used to drive the reset transistor, Q_1. The comparator output is also used as the "write" signal for the 8-bit, in-pixel memory. The memory is comprised of eight static latches, with a common bus for writing and reading the timing data. The 8-bit, in-pixel memory size was chosen as a compromise, between having sufficient resolution to assess the performance of the imager, and maintaining an acceptable fill factor for the pixel. Also, with testing in mind, 8-bit resolution greatly simplifies interfacing, storing and displaying of the image data. When reading data from the array, each pixel is addressed by a ROW and COL select lines, derived from the address decoders located at the periphery of the array. This places the pixel data on the data bus, which is then buffered to the chip output pins. The read operation is random, and nondestructive, allowing fast, repetitive access to the image data. The memory can be cleared prior to the next capture by placing null data on the bus, and pulsing V_{Ref} to V_C, which will force a write operation. To reduce idle power consumption, all voltage rails, except for V_{dd}, can be disabled between captures.

III. Time Domain ADC

A. Blanking and Linearization Operation

The previous section described the operation of the asynchronous pixel, and how the photocurrent is converted to a variable width pulse. The time from the start signal S_{Tint}, to the memory write signal will be referred to as the integration time T_{Int}. Two assumptions are made in deriving the ADC algorithm 1) the photocurrent I_{Ph}, is large enough to disregard other sources of leakage current and 2) I_{Ph} remains constant for the integration period. The junction capacitance is dependent upon voltage, and will be denoted as $C(v)$. A small variation in voltage dv results in a charge accumulation of dq

$$dq = I_{\mathrm{Ph}}dt = C(v)dv. \tag{1}$$

Integrating (1) for a period T_{Int}, corresponding to a voltage variation from V_{ref} to V_C, yields

$$I_{\mathrm{Ph}}T_{\mathrm{Int}} = \psi(V_C) - \psi(V_{\mathrm{ref}}) \tag{2}$$

where $\psi(V) = \int C(v)dv$. Therefore, the photocurrent I_{Ph}, is inversely proportional to the integration period T_{Int}

$$I_{\mathrm{Ph}} = \frac{\psi(V_C) - \psi(V_{\mathrm{ref}})}{T_{\mathrm{Int}}} = \frac{\alpha}{T_{\mathrm{Int}}} \tag{3}$$

where $\alpha = \psi(V_C) - \psi(V_{\mathrm{ref}})$.

The inverse relationship between the photocurrent and integration time must be compensated for by the ADC. If the photocurrent is to be quantized uniformly, the integration time must be quantized nonuniformly: small time steps for high photocurrents and large time steps for small photocurrents. This is achieved by adjusting the count rate as the integration period progresses. A down-counter is used, as the shortest integration time corresponds to the highest illumination (or photocurrent) in the scene. In order to determine the requirements of a time-based ADC, some limits have to be placed on the range of the conversion. Suppose the maximum photocurrent that is to be digitized is $I_{\max}$, which corresponds to the minimum integration time $T_{\min}$. The resolution of the conversion, ΔI, is determined by the size of the in-pixel memory

$$\Delta I = \frac{I_{\max}}{2^b - 1} \tag{4}$$

where b is the number of bits of the in-pixel memory. The smallest time step $\Delta T_{\min}$ is the difference between the integration times corresponding to $I_{\max} - \Delta I$ and $I_{\max}$:

$$\Delta T_{\min} = \frac{\alpha}{I_{\max} - \Delta I} - \frac{\alpha}{I_{\max}.}$$

Substituting for ΔI, using (4), and rearranging terms yields

$$\Delta T_{\min} = \frac{\alpha}{(2^b - 2) I_{\max}} = \frac{T_{\min}}{(2^b - 2)}. \tag{5}$$

Clearly, the dynamic range of the ADC (i.e., $I_{\max}$) can easily be controlled by simply varying the minimum time step size, $\Delta T_{\min}$: decreasing the minimum time step size increases the dynamic range and vice versa. In other words, the time-based ADC has a programmable dynamic range.

The timing counter must be driven at a frequency high enough to resolve the smallest time step $\Delta T_{\min}$. The smallest clock frequency that achieves this is referred to as the primary clock frequency, $F_{\mathrm{Pri}} = 1/\Delta T_{\min}$. It follows from (5) that the primary clock frequency is given by

$$F_{\mathrm{Pri}} = \frac{2^b - 2}{T_{\min}} = (2^b - 2)\frac{I_{\max}}{\alpha}. \tag{6}$$

It can be seen from (6) that the range of photocurrents, and hence the range of illumination over which the ADC operates, can be adjusted by varying the primary clock frequency F_{Pri}: increasing the primary clock frequency increases the range of the photocurrent. It should be noted that setting the maximum photocurrent by varying the primary clock frequency does not alter the pixel operation, this can only be achieved by varying V_C or V_{Ref}, see (2).

Since minimum integration time, corresponding to $I_{\max}$, $T_{\min} = (2^b - 2)\Delta T_{min}$, the ADC conversion counter should only start after $(2^b - 2)$ clock cycles. In other words, the conversion process must be suppressed or "blanked' for a period T_{Blank} equal to $(2^b - 2)$ clock pulses, after the integration period begins. If the blanking period is not applied, only photocurrents higher than $I_{\max}$ can be digitized. Fig. 3 shows a simulated ADC response with a primary clock frequency F_{Pri} set for an $I_{\max} = 55$ pA. Here, the range of the photocurrent is 100 pA, but obviously in a real scene the range may far

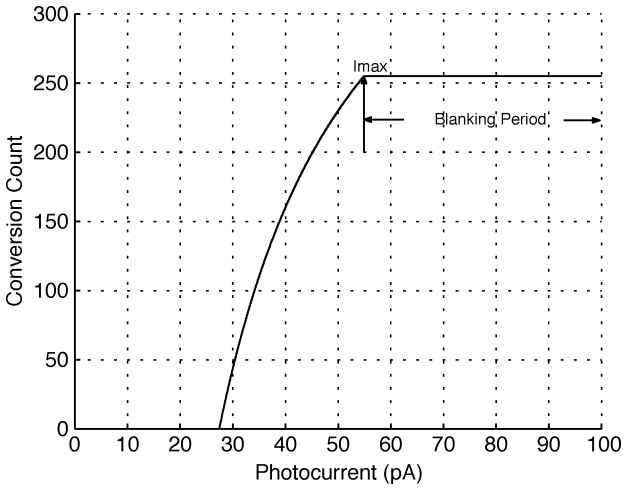


Fig. 3. Simulated ADC response using a fixed clock frequency and a blanking period set for a maximum photocurrent $I_{\max} = 55$ pA.

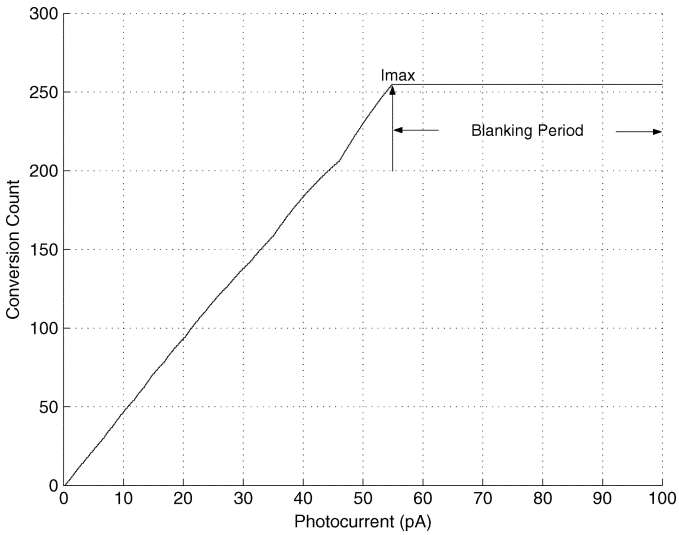
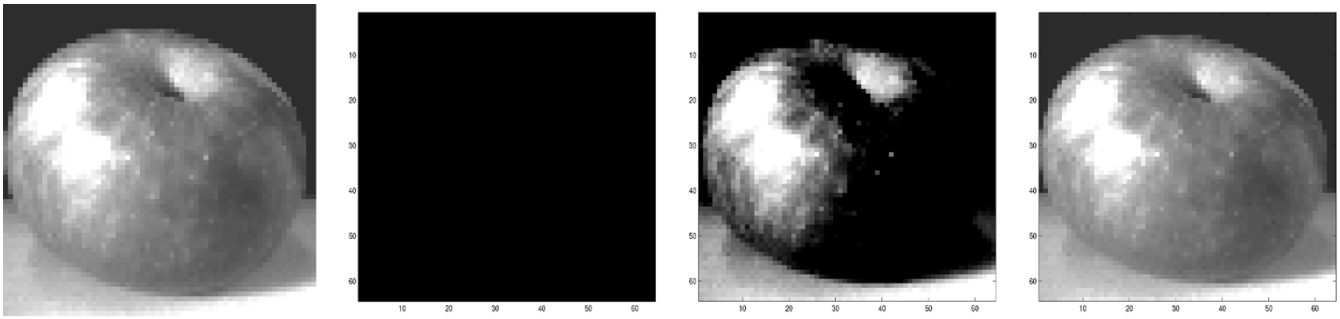


Fig. 4. ADC response using a variable frequency clock with a blanking period set for a maximum photocurrent $I_{\max} = 55$ pA.

exceed these limits. Pixels under high illumination will still operate, and store the timing data, however if this occurs to the right of $I_{\max}$, the Gray counter output, used to encode the digitized values, will remain static. It is only after the end of the blanking period that the Gray code data changes, and the different illumination levels are resolved (noting that as I_{Ph} and T_{Int} are inversely proportional, time progresses from right to left in Fig. 3). While the pixels themselves have a very wide operating range, the dynamic range of the captured image is always limited by the size of the in-pixel memory (i.e., number of bits). It can be seen from Fig. 3 that with a fixed clock the count reaches zero with only half of the current range digitized, resulting in the pixel memory being inefficiently utilized. To overcome this, a variable frequency clock must be used.

It was shown previously (3) that the relationship between the integration time and the photocurrent is nonlinear. Therefore, if the in-pixel memory is to be used efficiently, the ADC must compensate for this nonlinearity. This is accomplished by adjusting the frequency of the conversion clock as the conversion period progresses, using the value of the conversion data (the



(a) (b) (c) (d)

Fig. 5. Time domain ADC simulation results. (a) Input: 8-bit, grayscale image. (b) ADC output with a fixed clock and no blanking period. (c) ADC output with a fixed clock and blanking period. (d) Simulation output, variable clock, with blanking period.

counter output) as an index, that will determine the clock frequency at any time. By differentiating the integration time $T_{\rm Int}$ with respect to the photocurrent $I_{\rm Ph}$, see (3), we can establish the relationship between the conversion time step, $\Delta T_{\rm Conv}$, and the photocurrent quantization step, ΔI

$$\Delta T_{\rm Conv} = -\frac{\alpha}{I_{\rm Ph}^2}\Delta I = -\frac{\alpha}{N^2 \Delta I} \tag{7}$$

since $I_{\rm Ph} = N\Delta I$, $N = 0, \ldots, 2^b - 1$. Substituting for ΔI using (4) and for $I_{\max}$ using (6), we can express the conversion time step in terms of the primary clock frequency

$$\Delta T_{\rm Conv} = \frac{(2^b - 1)(2^b - 2)}{F_{\rm Pri} N^2}. \tag{8}$$

If the period of the clock driving the counter changes at the same rate as the integration time, a linear relationship between the count and the integration time will be maintained. This variable frequency clock can be expressed as a function of the counter output and the primary clock value as

$$F_{Var}(N) = \frac{1}{\Delta T_{\rm Conv}} = \frac{F_{\rm Pri} N^2}{(2^b - 1)(2^b - 2)}. \tag{9}$$

In practice, the variable clock $F_{Var}(N)$ is derived from the fixed primary clock$F_{\rm Pri}$, and a digital frequency divider circuit, with the divisor value being determined from a lookup table, using N as an index. The lookup table contains the divisor values, which will be referred to as M, derived from (9), such that

$$M(N) = \frac{N^2}{(2^b - 1)(2^b - 2)}. \tag{10}$$

There are two important considerations when generating the values of M contained in the lookup table. Firstly, the frequency division circuit can only divide the primary frequency by integer values, which leads to an error between the desired values of M, and the realizable values. Secondly, to simplify the hardware design, it is preferable to have less than the $(2^b - 1)$ possible values of M in the lookup table. Therefore, for a range of index values bounded by $N_{\rm Lo}$ and $N_{\rm Hi}$, a single value of M is used, calculated at the index value N_A. The approximated multiplier will be termed M_A, such that

$$M_A = \frac{N_A^2}{(2^b - 1)(2^b - 2)}, \quad N_{\rm Lo} < N > A < N > \text{Hi}. \tag{11}$$

The error between M and M_A, over the range bounded by $N_{\rm Lo}$ and $N_{\rm Hi}$, is termed e_A, and is given by

$$e_A(N) = \frac{N^2 - N_A^2}{(2^b - 1)(2^b - 2)}, \quad N_{\rm Lo} \le N \le N_{\rm Hi}. \tag{12}$$

The timing process is fundamentally one of counting clock periods from the time the conversion begins, with e_A representing the difference between the desired, and the achievable clock periods. As the Gray counter counts down from $N_{\rm Hi}$ to $N_{\rm Lo}$ these errors sum to give the total error over the range E_A

$$E_A(N) = \sum_{N=N_{\rm Hi}}^{N_{\rm Lo}} \frac{N^2 - N_A^2}{(2^b - 1)(2^b - 2)}, \quad N_{\rm Lo} \le N \le N_{\rm Hi}. \tag{13}$$

It can be seen from (12) that if $N_A > N$ the error is positive, and if $N_A > N$, the error is negative. It should therefore be possible to select a value of N_A (and therefore the values of M_A derived from (11)) such that the total error E_A, sums to zero over each range of values. In practice this results in a compromise between the maximum allowable error, which occurs at $N = N_A$, and the number of entries in the resulting lookup table. The values for $N_{\rm Lo}$, $N_{\rm Hi}$, and N_A were calculated iteratively in software, alternately placing limits upon the maximum error magnitude, and the number of table entries. This resulted in an acceptable compromise between performance and hardware complexity of 28 lookup table entries, which represents a significant saving in hardware requirements. Fig. 4 plots a simulation of the linearized ADC process, using the approximated values. While this result is applicable to the linearization algorithm similar techniques can be applied to produce more nonlinear, or piecewise linear ADC responses.

B. Simulation Results

During the design process the ADC was simulated in software, using 8-bit, grayscale, bitmap images as input. These are converted to 2-D matrices of integration times, using the inverse relationship between the photocurrent and the integration time in (3) (with appropriate values of $I_{\rm Ph}$ and α). Each "integration time" in the matrix is then digitized by simulating the conversion clock, blanking period, and the linearization algorithm in software.

Fig. 5 shows the images resulting from applying the time-based ADC conversion using the image in Fig. 5(a) as input. Driving the conversion counter with a fixed clock and without a blanking

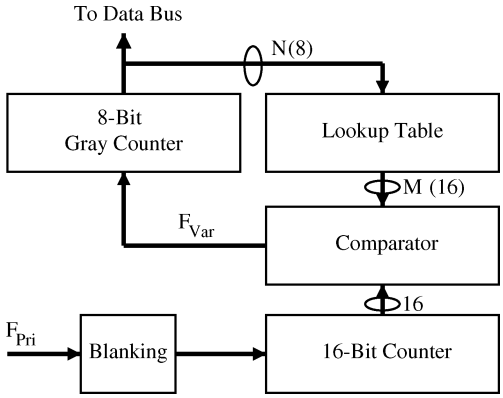


Fig. 6. Control circuit block diagram.

period results in Fig. 5(b) The conversion digitizes only the brightest points of the input image (although this is not obvious in the figure). Applying a blanking period results in the output of Fig. 5(c), which demonstrates the limited dynamic range of the fixed clock conversion. Using blanking and the linearization algorithm (with the approximated divisor values) produces Fig. 5(d). Performing the simulation with the 28 approximated ranges for the lookup table results in between 1 and 3 dB improvement in the signal to noise ratio (SNR), when compared with using all 255 possible values for M. The reason for the improvement is that the errors which occur due to the use of integer values of M, particularly in the early stages of the conversion, are controlled and never allowed to accumulate beyond set limits. Simulating the conversion scheme is very useful for confirming the ADC response prior to the hardware implementation.

IV. VLSI Implementation

A. Control Circuit Design

Fig. 6 is a block diagram of the control circuit, which realizes (9). While the derivation of the linearization process in the previous section appears complex, the hardware required to perform the algorithm is straightforward. As the DPS presented in this paper contains an 8-bit memory, the following description applies to an ADC where $b = 8$. The blanking circuit blocks the clock signal for 254 clock cycles, using an 8-bit counter and decoding logic. After blanking, the clock signal then drives a frequency divider circuit, constructed from a 16-bit counter, a magnitude comparator, and a lookup table. The 16-bit counter increments until the count is equal to the lookup table divisor value, when it will reset, and generate a clock pulse for the Gray counter. The output from the Gray counter is fed back to the frequency divider, as the index to the lookup table. In this way, (9) is realized on chip, with the only external control required being the selection of the initial clock frequency. As all of the system timing is derived from this one source, the ADC can be adapted to different conditions by varying F_{Pri} [see (6)]. The control circuit is a full custom design, and was simulated up to an operating frequency of 50 MHz, well above the anticipated operating requirements of the device. Several test circuits are also included below the array, which provide access to intermediate points in the pixel circuits. These circuits are used to test and characterize the analogue and digital performance of the pixel components.

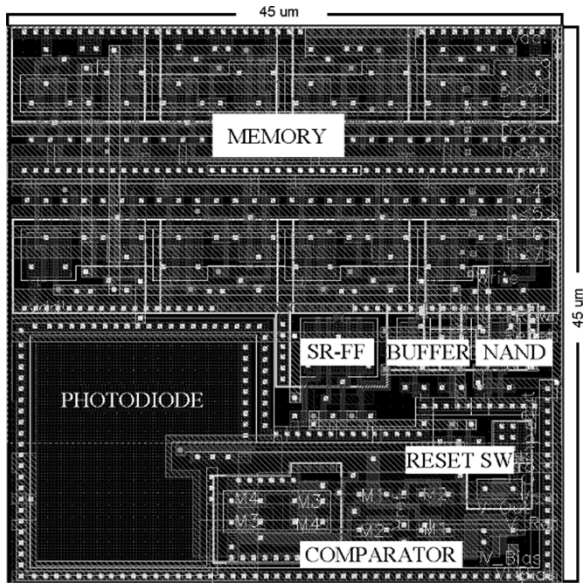


Fig. 7. Pixel layout, showing the main component parts.

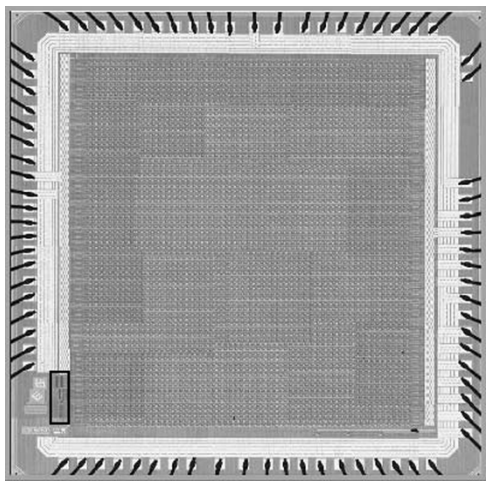


Fig. 8. Microphotograph of the 64 × 64 pixel array, with the control circuit highlighted. The control circuits occupies less than 0.5% of the total chip area.

Additional access is also provided to the internal data bus, so that the on-chip control circuit can be bypassed for testing, or more importantly, for implementing alternative ADC strategies.

B. Pixel Layout

The array of 64 × 64 pixels was manufactured in the Alcatel 0.35 μm, 3.3 V, digital CMOS process. This is a twin-tub, single-poly, five-metal, standard CMOS process. The pixel layout is shown in Fig. 7, with the major components labeled. The pixel is a mixed signal design, with analogue and digital components in close proximity. Power for the pixel is separated into 3.3 V digital (V_{dd}) and analogue (V_{dda}) supplies, with the comparators having a separate supply for bias (V_{Bias}). Guard rings (n-active/n-well to V_{dd}, p-active/p-well to gnd) are used extensively to prevent substrate coupling within the pixel, and between adjacent pixels. The entire pixel array is also surrounded by a guard ring, to screen it from peripheral digital circuits, such as buffers, address decoders, and the control circuit. The analogue comparator layout employs some basic rules for

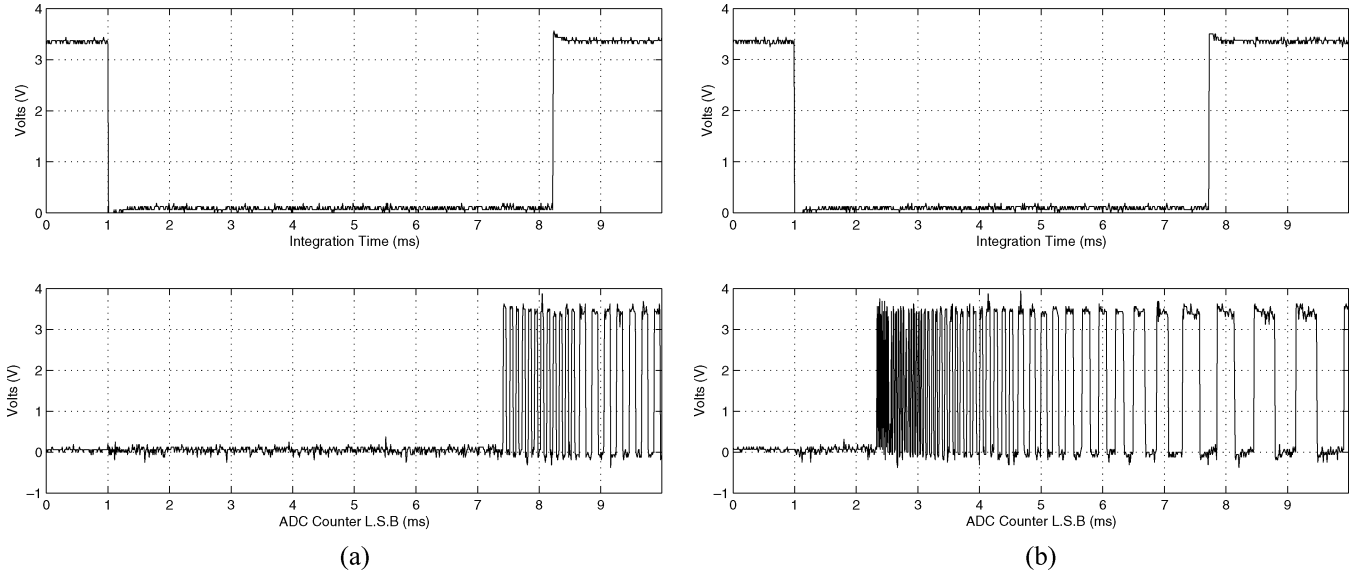


Fig. 9. Experimental measurement of the integration time and ADC counter LSB output for two different settings. (a) Integration time (top) and control circuit output data "B0' (bottom) operated at a primary clock frequency of 60 kHz. (b) Integration time (top) and control circuit output data "B0' (bottom) operated at a primary clock frequency of 200 kHz.

matching the devices in the differential stage: common centroid configuration, large device geometry (transistor width (W) and length (L) are 3 to 4 times λ), $W/L < 5$, and signal paths are matched in length and the number of vias. Each pixel measures 45 $\times$45 μm, and the control circuit measures 140 $\times$470 μm. The complete chip occupies an area of 3.9 $\times$ 3.7 mm, a microphotograph of which is presented in Fig. 8. The control circuit is highlighted at the bottom left-hand side of the image. The die is mounted in a PLCC84 carrier.

V. Testing and Experimental Results

A. Test Setup

The array is mounted in a custom PCB which provides the required analogue and digital voltage rails ($V_{\rm dd}$, $V_{\rm dda}$, V_C, and $V_{\rm Bias}$). A RISC micro-controller interfaces between the array and a PC (running the Linux operating system) via the PC parallel port, which limits the data transfer rate to approximately 80 kbytes/s, currently only supporting still image capture. A digital light meter (also under PC control), in conjunction with an integrating sphere, is used to characterize the performance of the imager (ADC response, FPN, and dark current). When generating the programmable timing data off-chip, the ADC algorithm lookup table is held in the firmware of the micro-controller. Images are focused onto the array using a variety of "board mount" lenses, and all images presented in this paper are read directly from the array, without any post-processing.

B. Test Results

Single pixel characteristics were determined using the pixel test circuits at the periphery of the array. Figs. 9 and 10 show the progression of signals as they occur in an image capture. Fig. 9 (top) is the SR "Q' output showing the PWM signal, T_{int}. Fig. 9 (bottom) represents the plot of data bit "B0', clearly showing the blanking period and the variable frequency clock, synchronized with T_{int}. Fig. 9 also illustrates how the primary clock signal

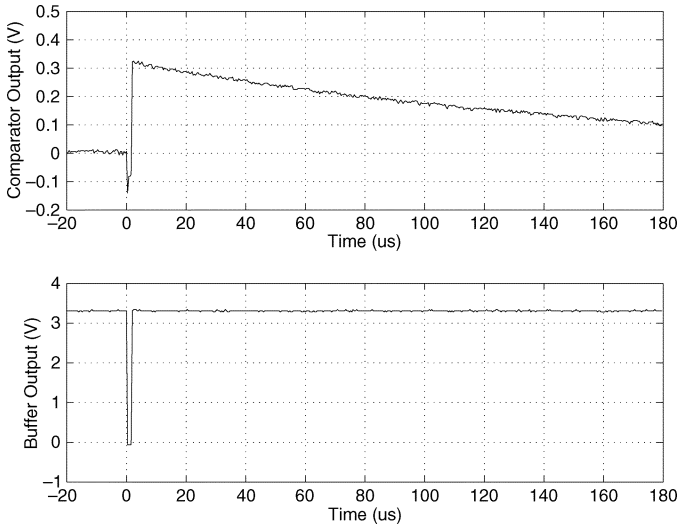


Fig. 10. (Top) Comparator output and (bottom) memory write signal, taken from the pixel test circuits.

is used in order to calibrate the sensor response according to the level of illumination. The setup example shown on Fig. 9(b) presents a faster modulation frequency and a reduced blanking time as compared to the setup of Fig. 9(a), which is more appropriate for high illumination conditions. Fig. 10 is the output from a test circuit comparator (top) and the memory write signal taken from the first inverter stage of the buffer (bottom). (Note that the comparator signal has been distorted by the loading of the test pin). The dark current places a lower limit on the effective operation of the pixel, and the ADC algorithm. As the pixel capacitance can only ever be estimated, it is considered more appropriate to express the dark current as the *dark voltage rate*. The integration time was measured with zero illumination ($V_C - V_{\rm Ref} = 0.4$ V) over several chips, with the *mean dark time* (MDT) equal to 41 s, which results in a mean dark rate of 9.8 mV/s. It must be noted that definitions for industry

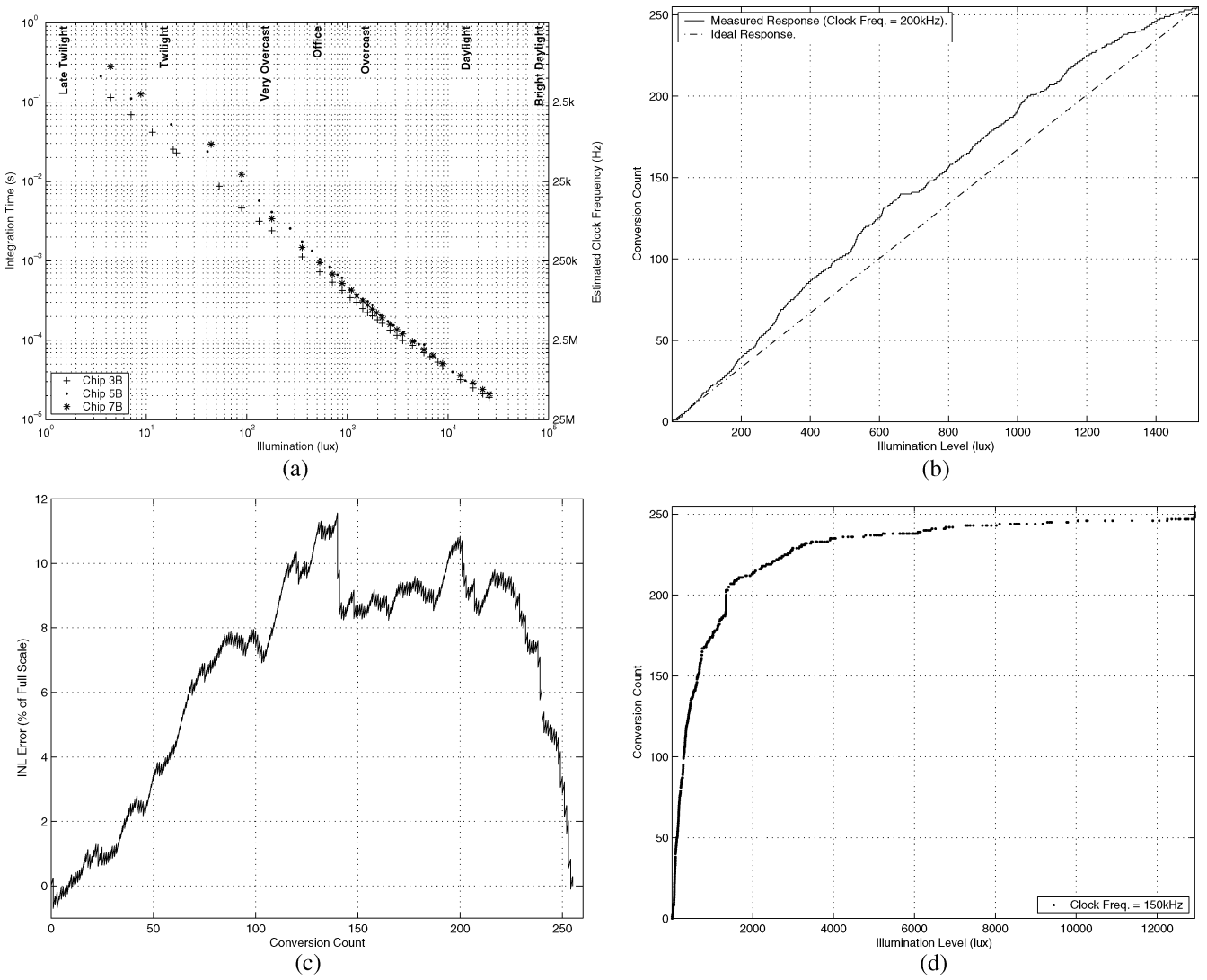


Fig. 11. Experimental results. (a) Integration time and primary clock frequency versus illumination. (b) Linearized ADC response. (c) Linearized ADC response INL. (d) Wide dynamic range response.

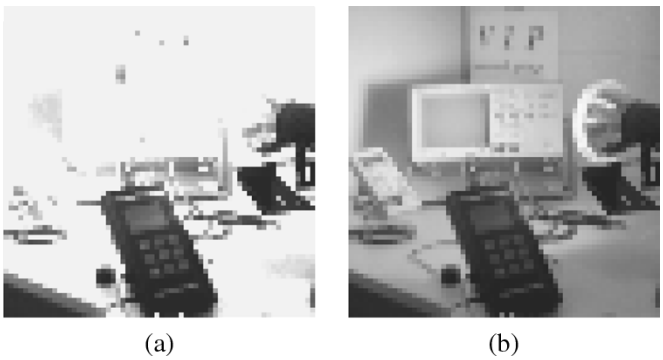


Fig. 12. Wide dynamic range image capture. (a) Image capture using a linear ADC response. (b) Image capture with the nonlinear ADC response.

TABLE I
SUMMARY OF THE CHIP FEATURES

Technology	Alcatel 0.35μm, 5 metal, single-poly, twin well, CMOS
Supply Voltage	3.3V
Comparator bias voltage	0.35V
Pixel dynamic operating range	$> 100dB$
ADC dynamic range (linear mode)	$48dB$
Mean dark time	41s
Mean dark rate	9.8mV/s
FPN	0.8%
Average power	$1.6\mu A$ per DPS
Pixel area	45μm$\times 45\mu$m
Die area	3.7mm$\times$3.9mm
Package	PLCC84

standard measurements such as dynamic range, noise equivalent exposure (NEE) and saturation equivalent exposure (SEE) are difficult to apply to the pixel/ADC operation, as these tend to be voltage based measurements, and in this pixel the operating voltage range is always constrained between V_C and V_{Ref}. For this reason we have presented our results as plainly as possible, while avoiding the use of terms which may be misinterpreted. When considering the dynamic range of the array, three

(a) (b) (c)

Fig. 13. Image capture operation under different settings, confirming earlier ADC simulations. (a) Image capture, fixed clock, no blanking. $F_{\mathrm{Pri}} = 3$ kHz. (b) Image capture, fixed clock, with blanking. $F_{\mathrm{Pri}} = 3$ kHz. (c) Image capture, variable clock, with blanking. $F_{\mathrm{Pri}} = 3$ kHz.

distinct areas must be considered: 1) the PWM circuit operation, 2) the in-pixel memory, and 3) the wide dynamic range response. Firstly, the PWM circuit within each pixel generates a pulse which is inversely proportional to the illumination, and even given certain constraints, such as the design assumptions regarding dark current, it exhibits a very wide operational range. As this is a time based system, we have taken the dynamic range (DR) of the pixel as the ratio of the maximum integration time (as determined by the dark current assumptions, see Section III), and the experimentally determined minimum integration time, as

$$DR = 20log\left(\frac{T_{\mathrm{Int(max)}}}{T_{\mathrm{Int(min)}}}\right). \tag{14}$$

Fig. 11(a) shows integration times measured from the test pixel, and the primary clock frequency required for a linearized conversion, for five decades of illumination. While the light source used to produce Fig. 11(a) had insufficient range to completely saturate the pixel, testing showed that integration times of 10 μs were possible, resulting in a theoretical dynamic range for the pixel of 100 dB. Secondly, due to the constraint of the 8-bit, in-pixel memory, there is an absolute limit on a linearized conversion of 48 dB. Finally, if the nonlinear response is used, a much wider range of levels may be captured, but this comes at the expense of conversion resolution. The response presented in Fig. 12, represents a moderate compression, extending the intrascene range. The response may be tailored to suit the application, and is limited only by the operation of the pixel. The linearity of the conversion was measured by flat-field illuminating the array and varying the intensity of the illumination through the full digital range of the ADC, resulting in the plot of Fig. 11(b). The endpoint line for INL measurements is included for reference. The integral nonlinearity (INL) plot (using the straight line endpoint reference) is shown in Fig. 11(c). The INL plot shows that the algorithm for determining the lookup table had successfully prevented the uncontrolled accumulation of rounding errors. An overall improvement in the INL could be achieved by increasing the resolution of the digital frequency division circuit, or replacing it with a more complex method for realizing (10). It was considered that this was not warranted at this stage, due to the relatively small size of the array. Demonstrating the programmability of the ADC response, Fig. 11(d) is a plot of the wide dynamic range response. Using the same device but altering the data timing, the response now compresses a wide range of illumination into the top 20% of the digital values. Again, note that the test setup was unable to saturate the array. Fig. 12 demonstrates the effect of producing an image using this dynamic range compression. The illumination levels in the scene range from the foreground in office light, to a background brightly lit by a spotlight (at the right of the scene). Fig. 12(a) is captured using a linearized ADC response, with most of the image overexposed. The same scene is captured in Fig. 12(b), with nonlinear response, revealing the previously overexposed areas. Dynamic range compression clearly demonstrates the potential of the proposed technique in overcoming the limited dynamic range imposed by the 8-bit conversion in our DPS.

The average current per DPS was measured at about 1.6 μA. The resulting power consumption can be divided into three components: power consumed by the digital circuit (memory and SR latch), power consumed by the chargeup of the sensing node, and finally power consumed by the analog comparator, representing 75%, 17%, and 8%, respectively. The chargeup power is kept quite low (17%) in our approach as the self-resetting operation prevents the total discharge of the sensing node using the SR latch. The charge-discharge swing is kept constant and equal to $V_C - V_{\mathrm{ref}}$ for all pixels within the array.

Since an asynchronous reset approach is adopted, the power consumed is spread over time and large peak currents typically experienced during the reset phase of conventional architecture is avoided. In addition, in contrast to the spiking pixel architecture [7], only a single pulse (PWM) is used in our approach in order to encode the photocurrent which results in further power saving. The average current of the spiking pixel was reported to be 132.8 μA per pixel with no on-pixel memory [7], compared to 1.6 μA of our sensor with on-pixel memory. The FPN was measured by uniformly illuminating the array (without a lens or lens mount) using the integrating sphere and capturing the flat field image. This is repeated 200 times for each chip and the resulting images averaged, to remove any temporal variations. The FPN appears mainly as a fixed voltage offset, we believe due to reset noise, and mismatch in the first comparator stage. It was found that the level of FPN was dependent upon the voltage range $V_c - V_{\mathrm{Ref}}$, and that a voltage range of at least $V_C - V_{\mathrm{Ref}} = 0.8$ V was required for an FPN level of less than 0.8%. This result was obtained without any additional reduction strategies (such as correlated double sampling). It has been shown that FPN levels

(a) (b) (c)

Fig. 14. Sample images acquired from the 64 × 64 sensor prototype. (a) Vision lab. (b) Oscilloscope and meter image. (c) Po image.

of this level, although discernable to the human eye, are acceptable for the low level imaging applications intended for this imager [15]. This level could have been reduced further, through digital correction techniques, however it was considered more appropriate to the philosophy of a stand alone, proof-of-concept device, to accept this as a factor in the development of processing algorithms, until a workable FPN reduction strategy could be incorporated into future designs. Table I summarizes the performance and features of the prototype DPS array. Fig. 14 shows some sample images acquired from the DPS array prototype. One should note that all sample images included in this paper are presented "as read' from the array, with no FPN correction or further processing applied. The simulations of the ADC operation displayed in Fig. 5 were repeated using the manufactured array, and are shown in Fig. 13. The effects of the various timing parameters are more obvious in the real images than in the software simulations. In particular, Fig. 13(a) shows that only the brightest levels in the scene are resolved when operating the ADC with a simple, fixed clock. Fig. 13(b) demonstrates the improvement when including a blanking period, and how the limited dynamic range of the nonlinear transfer characteristic makes poor use of the 8-bit memory.

VI. Conclusion

This paper introduced a DPS array, in which the pixel response is digitized using a time domain ADC. We have proposed a novel pixel architecture based on an asynchronous self-resetting mode, which has the advantage, over the synchronous self-resetting mode, of avoiding large peak by using a start integration signal as a reset, instead of a global reset signal. The nonlinear relationship between the photocurrent and the integration time found in pulsewidth based converter is linearized by an on-chip digitally programmable frequency divider, which generates Gray-coded data that is stored in pixel memory. This results in a novel digital control of the imager, adapting to different lighting conditions by varying a single clock frequency. Interesting features such as dynamic range compression were also experimentally demonstrated which clearly shows the potential of the proposed technique in overcoming the limited dynamic range typically imposed by the number of bits in a DPS. A 64 × 64 pixel array has been manufactured in a commercial 0.35 μm CMOS process, and found to be fully functional. Experimental results showed a 100 dB dynamic range, a 41 s mean dark time and an average current of 1.6 μA per DPS.

References

[1] E. Fossum, "CMOS image sensors: electronic camera on chip," *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1689–1698, Oct. 2001.

[2] A. B. Wandell, A. El Gamal, and B. Girod, "Common principles of image acquisition systems and biological vision," *Proc. IEEE*, vol. 90, no. 1, pp. 5–17, Jan. 2002.

[3] D. Yang, B. Fowler, and A. El Gamal, "A Nyquist-rate pixel-level ADC for CMOS image sensors," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 348–356, Mar. 1999.

[4] S. Kleinfelder, S. H. Lim, X. Q. Liu, and A. El Gamal, "A 10 000 frames/s 0.18 μm CMOS digital pixel sensor with pixel-level memory," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, Feb. 2001, pp. 88–89.

[5] ——, "A 10 000 frames/s CMOS digital pixel sensor," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2049–2059, Dec. 2001.

[6] A. Bermak, A. Bouzerdoum, and K. Eshraghian, "A vision sensor with on-pixel ADC and in-built light adaptation mechanism," *Microelectron. J.*, vol. 33, no. 12, pp. 1091–1096, 2002.

[7] J. Doge, G. Schonfelder, G. T. Streil, and A. Konig, "An HDR CMOS image sensor with spiking pixels, pixel-level ADC, and linear characteristics," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 2, pp. 155–158, Feb. 2002.

[8] A. Uehara, K. Kagawa, J. Tokuda, T. Ohta, and M. Nunoshita, "Backilluminated pulse-frequency-modulated photosensor using silicon-onsapphire technology for use as epi-retinal prosthesis device," *Electron. Lett.*, vol. 39, no. 15, p. 11 021 104, Jul. 2003.

[9] E. Culurciello, R. Etienne-Cummings, and K. A. Boahen, "A biomorphic digital image sensor," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, p. 281 294, Feb. 2003.

[10] W. Yang, "A wide-dynamic-range, low-power photosensor array," in *Proc. ISSCC*, San Francisco, Feb. 1994, p. 230 231.

[11] A. Bermak, "A CMOS imager with PFM/PWM based analog-to-digital converter," in *Proc. Int. Symp. Circuit Systems*, vol. 4, 2002, pp. 53–56.

[12] X. Qi, X. Guo, and J. G. Harris, "A time-to-first spike CMOS imager," in *Proc. Int. Symp. Circuit Systems*, vol. 4, 2004, pp. 23–26.

[13] A. Kitchen, A. Bermak, and A. Bouzerdoum, "PWM digital pixel sensor based on asynchronous self-resetting scheme," *IEEE Electron Device Lett.*, vol. 25, no. 7, pp. 471–473, Jul. 2004.

[14] G. P. Weckler, "Operation of p-n junction photodetectors in a photon flux integrating mode," *IEEE J. Solid State Circuits*, vol. 2, no. 3, pp. 65–73, Sep. 1967.

[15] R. Etienne-Cummings, Z. K. Kalayjian, and D. Cai, "A programmable focal-plane mimd image processor chip," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 64–73, Jan. 2001.

Alistair Kitchen (S'04) received the B.S and M.S degrees in electronic engineering from Edith Cowan University, Joondalup, Australia, in 2002 and 2004 respectively, where he is currently pursuing a Ph.D. degree, researching high-speed CMOS photodetectors for optical interconnects.

His research interests include intelligent pixels, CMOS photodetectors, interchip and intrachip optical interconnects.

Mr. Kitchen is a recipient of the Institution of Engineers Australia, Electrical College Prize, and the IEE prize for Academic Achievement.

Amine Bermak (M'99–SM'04) received the M.Eng. and Ph.D. degrees in electronic engineering from Paul Sabatier University, Toulouse, France in 1994 and 1998, respectively.

During his Ph.D. studies, he was part of the Microsystems and Microstructures Research Group at the French National Research Center LAAS-CNRS where he developed a 3-D VLSI chip for artificial neural network classification and detection applications. He joined the Advanced Computer Architecture Research Group at York University, U.K., where he was a Post-doctoral Researcher on VLSI implementation of CMM neural networks for vision applications in a project funded by British Aerospace. In November 1998, he joined Edith Cowan University, Perth, Australia, first as a Research Fellow working on smart vision sensors, then as a Lecturer and a Senior Lecturer in the School of Engineering and Mathematics. He is currently an Assistant Professor with the Electrical and Electronic Engineering Department of Hong Kong University of Science and Technology (HKUST), Kowloon, where he is also serving as the Associate Director of Computer Engineering Program. His research interests are related to VLSI circuits and systems for signal, image processing, sensors and microsystems applications. He has published extensively on the above topics in various journals, book chapters and refereed international conferences. He has published more than 70 papers in journals, book chapters, and refereed international conferences.

Dr. Bermak received the "Early Career Researcher Award" from the Australian Academy of Science in 2002. In 2004, he was awarded the "School of Engineering Teaching Excellence Award." He is the recipient of the best paper award at the 2005 5th IEEE International Workshop on System-on-chip for Real-Time Applications . He is a member of IEEE CAS committee on sensory systems.

Abdesselam Bouzerdoum (M'89–SM'03) received the M.S. and Ph.D. degrees, both in electrical engineering, from the University of Washington, Seattle.

He joined the University of Adelaide, Adelaide, Autralia, in July 1991, and in 1998 he was appointed Associate Professor at Edith Cowan University, Perth, Australia. Since 2004 he has been with the University of Wollongong, NSW, Australia, where he is currently Professor of Computer Engineering and Head of School of Electrical, Computer and Telecommunications Engineering. From May to June 2004, he was a Visiting Professor at Institut Galile, University of Paris, Paris, France. He has published over 200 technical articles and graduated 13 Ph.D. and 6 M.S. degree students. His research interests include signal/image processing, pattern recognition, machine learning/neural networks, and VLSI implementation of smart vision micro-sensors.

Dr. Bouzerdoum has received several fellowships and distinguished awards; among them are the Vice Chancellors Distinguished Researcher Award in 1998 and 1999, and the Awards for Excellence in Research Leadership and Excellence in Postgraduate Supervision. In 2001 he was the recipient of a Distinguished Researcher (Chercheur de Haut Niveau) Fellowship from the French Ministry of Research to spend three months at the National Research Centre LAAS—CNRS in Toulouse. Dr. Bouzerdoum served as Chair of the IEEE WA Section Signal Processing Chapter in 2004, and was Chair of the IEEE SA Section NN RIG from 1995 to 1997. Currently, he is serving as Associate Editor for the IEEE TRANSACTIONS ON SYSTEMS, MAN AND CYBERNETICS. He is a member of the INNS, and a member of IASTED Technical Committee on Neural Networks.