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Dynamic Spot Generation Using Opto-VLSI Processing

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Abstract:

In this paper we demonstrate the capability of Opto-VLSI processors to generate arbitrary optical power distribution for adaptive optical beam splitting and dynamic optical spot generation. By using the multicasting capability of Opto-VLSI processors, an input optical signal can be dynamically split into N spots array, and the output power of each spot can be independently configured. Experimental results of multiple beam splitting show that dynamic optical multicasting can be achieved with more than 20dB dynamic range. Special patterns are also generated by optimising the phase hologram of the Opto-VLSI processor to place the output beam spots at appropriate positions.

1. Introduction:

Diffraction optical elements that multicast single laser source are essential components for dynamic optical access network and reconfigurable parallel computing architectures. In these systems, great advantages can be gained if the intensity of the input beam is dynamically split according to a reconfigured weight matrix [1, 2].

Many passive and active structures have been developed to realise dynamic optical splitting [3-7]. While passive optical splitters are adequate for current optical access networks, future services require reconfigurable optical splitters because they overcome the major flexibility limitation of static optical splitters encountered in existing optical networks. In a dynamic mode, a reconfigurable optical splitter can dynamically distribute the optical power without changing its physical configuration. This offers a more flexible and cost-effective option in comparison to passive optical splitters. A smooth migration from passive to totally dynamic optical splitters is therefore necessary for future reconfigurable optical networks [8].

Opto-VLSI processors have recently been demonstrated for realising dynamic optical power distribution [9]. An Opto-VLSI processor is an optical spatial phase modulator capable of achieving beam steering, focusing and multicasting. A typical Opto-VLSI processor consists of liquid crystal (LC) pixels driven by a Very-Large-Scale-Integrated (VLSI) circuit, each pixel can be driven by many discrete voltage levels thus generating phase holograms capable of performing adaptive optical beam steering/multicasting through quantized phase holograms uploaded onto the Opto-VLSI processor.

In this paper, we demonstrate the capability of Opto-VLSI processors to generate dynamic optical power splitting profiles. Improved simulated annealing (SA) algorithm is used to calculate the phase holograms that generate arbitrary output splitting profiles. Experiments are setup to generate proof-of-concept 1x3, 2x3, and 3x3 spots arrays. Output optical beams are coupled into output fibre ports by a piecewise linear optic to monitor output properties. Experimental results show more than 20dB dynamic range and good power distribution accuracy. Different spot arrays are generated at appropriate positions to form alphabet letters, which demonstrate the capability of Opto-VLSI processors to synthesise arbitrary spot patterns.

2. Improved Simulated Annealing Algorithm

The Opto-VLSI processor is driven by computer holograms generated using a simulated annealing (SA) algorithm [10], which first defines a cost function as a measure of the distance between the diffracted field pattern of a target output spot array and the field pattern of the current candidate hologram. The algorithm starts from an initial random hologram pattern, $h(x,y)$, and computes the resulting diffraction field represented by a Fourier transform. For a pixellated hologram, $h(m,n)$, the diffracted beam $H(k,l)$ is described by

$$H(k,l) \equiv \text{DFT}\{h(m,n)\} \quad (1)$$

where DFT denotes the discrete Fourier Transform, and (m,n) and (k,l) represent the coordinates in the hologram and output planes, respectively. A cost function is calculated as a measure of the discrepancy between the target spot array and the diffraction field of the hologram. Next, a pixel or a group of pixels are randomly changed (subject to the constraint on the phase levels), then the cost function is calculated again. Note that there is no need to recalculate the entire diffraction field $H(k,l)$, when changing a pixel: it will be possible to compute the change in diffraction field ΔH_T arising from the change in a single pixel $\Delta h_{m,n}$ as follows

$$\Delta H_T = \Delta h_{m,n} e^{-2\pi j(km+ln)/N} \quad (2)$$

This results in a change in cost function, ΔC . If the cost decreases (that is ΔC is negative), the pixel change is accepted, otherwise, the pixel is accepted with a probability of $e^{\Delta C/T}$, where T is the "temperature", which is gradually reduced as the number of iterations

increases. The evolution of the temperature as a function of the number of iterations is expressed as

$$T = T_o e^{-T_c i / I} \quad (3)$$

where T_o and T_c are parameters that determine the starting value and rate of decrease of the temperature, i is the current iteration number, and I is the total number of desired iterations. The end of the algorithm can be set at a certain number of iterations, or when the cost has been reduced to a determined level, or alternatively, when the temperature has been reduced to a certain value.

To reduce the time required for hologram generation and channel crosstalk, and most importantly to improve diffraction efficiency, we modified the algorithm by adding constraints on active pixel number (m, n) that only the pixels that encircle the diameter of the incident beam are used for hologram calculation, whereas all other pixels are masked with their phases set to zeros.

3. Experiment setup

In our experiments, a 40-micron pixel size, 128x128-pixel nematic LC Opto-VLSI processor was used and the input Gaussian optical beam was collimated to a beam diameter of 1mm so that the number of active pixel encircling the input optical beam was 50x50 (rather than the whole 128x128-pixel area of the Opto-VLSI processor), which has 2x2 mm² active area and covers more than 99% of the input optical power. The basic structure of the dynamic optical power splitter using Opto-VLSI technology is shown in Figure 1. It comprises an input fibre collimator, an Opto-VLSI processor, a three channel piecewise linear prism as an optical router, and an output fibre collimator array. The input optical signal is transformed, via the input collimating lens, into free-space collimated Gaussian optical beam with beam diameter about 1mm, which illuminates a 50x50-pixel block on the Opto-VLSI processor. The 50x50-pixel block is driven by a multicasting holographic diffraction grating, which is calculated based on the improved SA algorithm using MATLAB programs. The output spot patterns were directly captured by a CCD camera through a sampling mirror, and analysed by a Spiricon beam profile analyser. To couple the output beams into fibre ports, a fibre collimator array was used and connected to an Optical Spectrum Analyser (OSA) for power measurements. The role of the piecewise linear lens was to steer the diffracted split beams along parallel directions so that they can be coupled into the output fibre collimator array with high efficiency.

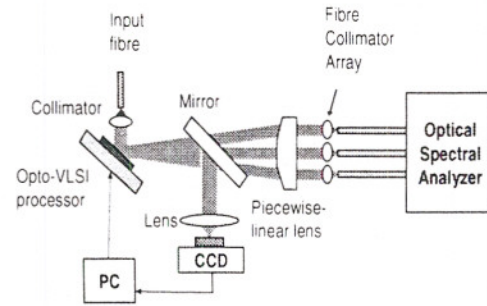


Fig.1 Experimental setup of dynamic power splitter using an Opto-VLSI processor

4. Experimental results:

A variety of holograms were generated to control the Opto-VLSI processor and demonstrate its capability to realize dynamic power splitting. Figure 2 shows the measured output spot arrays for an input optical beam that was dynamically split into (a) three uniform output spots with equal output power, (b) three spot array with one spot output power down to a half and the other spot powers kept unchanged (the beam spot to the right is the diffracted zeroth order beam, which has low power compared to the other output spots), (c) 2x3 spot array with uniform power distribution, (d) 3x3 spots array with uniform power distribution, and (e) 3x3 spots array with the centre beam removed. It is obvious from Figs 2(a)-(e) that the zeroth order beams have low power compared to the split spots, and are located at different positions than the split beams by properly defining their positions, hence they are not coupled into the output fibre ports. It is worthwhile noting that the position and power of each output spot can independently be adjusted by generating optimized phase holograms that produces the desired spot profiles.

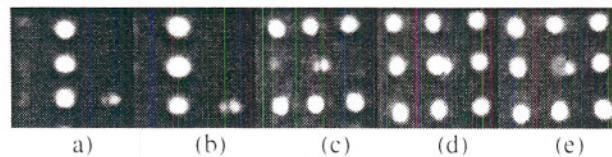


Fig.2 Dynamic spot array generation using Opto-VLSI processor.

Figure 3 shows the measured output power versus the normalized target power per channel for a three-channel splitter. A very good splitting uniformity is seen for normalized splitting ratios higher than 0.2. For lower splitting ratios, the splitting uniformity is slightly degraded due to the fact that the crosstalk becomes higher than the power of the split spots.

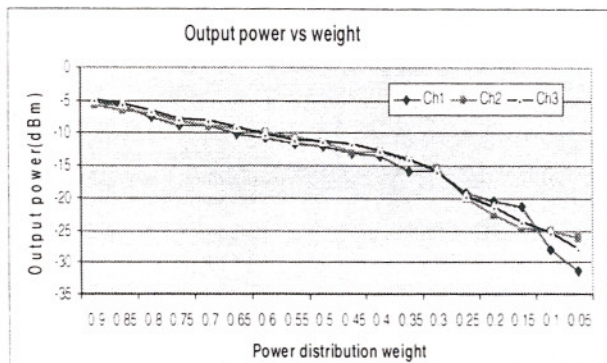


Fig.3 Measured three channel output power verses power distribution weight

By appropriately defining the output spot powers and spot positions, some special patterns can be generated at the output plane. Figure 4 shows the phase holograms and the corresponding patterns, which are the capital letters "E" "C" "U" "M" "P". It is obvious that arbitrary patterns can be generated using the simulated annealing algorithm.

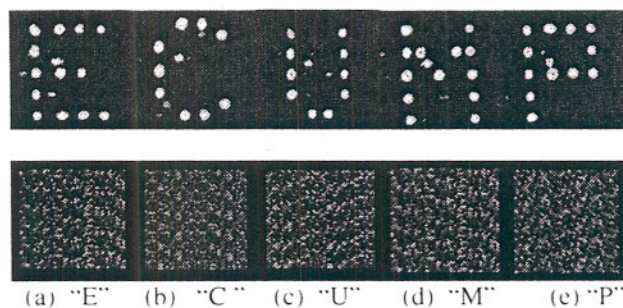


Figure 4 Holograms generating different capital letters.

5. Conclusion:

A dynamic optical power splitter based on a reconfigurable Opto-VLSI processor is presented in this paper. It can be used as an active beam splitter or special spot pattern generator. An improved simulated annealing algorithm is used to calculate the phase holograms using MATLAB Software, which enabled a much shorter programming time and a higher diffraction efficiency to be attained. Proof-of-concept reconfigurable 1:3 optical splitter that utilizes an Opto-VLSI processor to adaptively split optical signal into different output fibre ports has experimentally been demonstrated, and the results show more than 20dB dynamic range. Different output spots including alphabet letters with arbitrary weights at arbitrary positions have also been generated demonstrating the capability of Opto-VLSI processors to realise dynamic power multicasting.

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