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Oscillation Built-in-Self-Test for ADC Linearity Testing in Deep Submicron CMOS Technology

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Abstract

This paper proposes an Oscillation BIST (OBIST) that is meant to test ADCs fabricated in sub 100nm processes. The design is intended to be capable of testing a 10-bit ADC that was designed in 40nm CMOS. The design scheme presents a simple analog stimulus generator that was designed in 40nm CMOS together with schematic based simulation results. There is also a description of a calibration circuit and a high-level implementation of a BIST control system to run the BIST and to calculate static parameters such as Differential Non-linearity (DNL) and Integral Non-linearity (INL). Simulation results for the analog stimulus generator suggest that OBIST might still be a viable method to test ADCs despite device scaling to sub 100nm processes.

Keywords

Analog-to-Digital Converters, Analog-to-digital converter testing, Built-in Self Test, Oscillation BIST.

1. Introduction

Testing mixed signal components on a System-On-Chip (SoC) is costly due to the relatively long test time and the need to have analog testing capabilities on the Automatic Test Equipment (ATE). Hence, moving towards a low cost Built-In-Self-Test (BIST) solution to test mixed signal components to reduce test time and test costs is an attractive proposition. This paper presents an Oscillation BIST (OBIST) solution that is capable of testing a 10-bit successive approximation ADC with a nominal full-scale analog input voltage range of 2V. The difference of this BIST solution with previous literature on the same subject matter is that this solution is designed using CMOS 40nm deep submicron devices.

Previous literature on the OBIST has shown that the design of the on-chip analog saw-tooth waveform generator can be done in CMOS 1.2 μm technology [1]. Similar on-chip stimulus generators such as adaptive ramp generators have been implemented in 0.35 μm CMOS [2]. Since then, device scaling to lower nodes has given rise to more pronounced second order effects when designing circuits in CMOS. There is a lack of documentation in research literature regarding how these changes have impacted the feasibility of designing the on-chip analog signal generator for OBIST in sub 100nm processes.

The following sections in this paper will briefly discuss the test structure for OBIST, present a design and simulation of an on-chip analog signal generator to stimulate the ADC and finally discuss the theoretical implementation of a digital BIST engine that controls the test.

2. Oscillation BIST Overview

OBIST relies on generating a controlled analog input voltage that is forced to oscillate between 2 adjacent transition voltages in the ADC output code set. The resultant oscillation frequency is then converted to a number by a Frequency-to-Number Converter (FNC). Figure 1 depicts how the analog input waveform would theoretically oscillate between 2 adjacent transition voltages, V_{Tk}^{A} and V_{Tj+1}^{A}. The voltage interval between the 2 transition voltages denotes a quantization interval while the ADC conversion time is denoted by t_C.

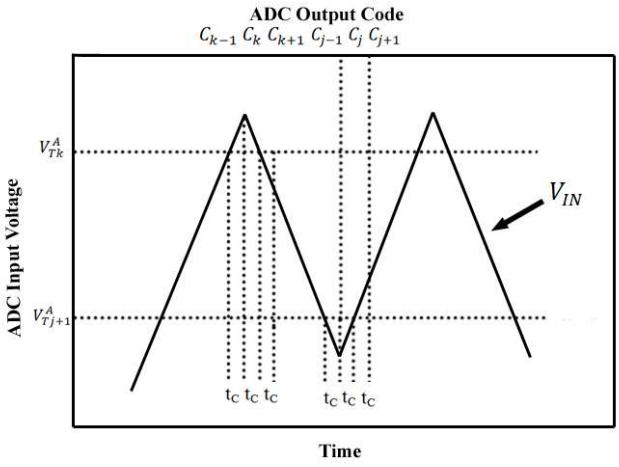

Figure 1: Analog input stimulus oscillating between 2 transition voltages for OBIST testing [1]

An example of an FNC that was implemented as presented in [1] is shown in Figure 2 where the LCD module is a level

crossing detector that converts the oscillation waveform into a continuous clock pulse waveform.

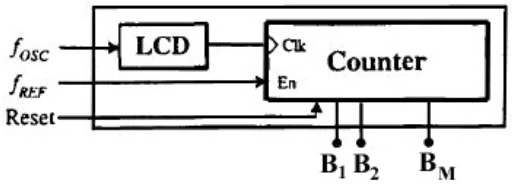

Figure 2: Frequency-to-number converter block diagram with level crossing detector (LCD) [1]

The output of the FNC is denoted by the counter output B in equation (1) and is a function of both the oscillation frequency and the reference frequency.

$$B_{LM} = \frac{f_{OSC}}{2 f_{REF}} \quad (1)$$

The measured deviation in oscillation frequency with respect to a nominal reference frequency is used to denote the DNL of a specific quantization interval for the ADC. A larger interval would result in a lower frequency and vice versa assuming the slew rate in the input signal is constant. The size of the quantization intervals in an actual ADC determines the resulting DNL for that interval. The DNL for the n^{th} ADC output code is expressed in equation (2) where Q_A is the actual quantization interval and Q_N is the ideal quantization interval in terms of LSB.

$$DNL(n) = \frac{Q_A - Q_N}{Q_N} \quad (2)$$

The advantage of having a frequency based DNL measurement is that there is no need to fulfill a linearity requirement to test ADCs. For example, a common method used to determine the DNL of an ADC involves histogram testing where a ramp, triangle wave or sine wave input stimulus is typically required to have at least 2-bits higher linearity than the ADC under test [3]. This constraint has made it difficult to build small and low cost on-chip analog signal generators with high linearity especially when testing ADCs with 10-bits or more resolution. A frequency based measurement would now rely on how accurately we are able to measure the frequency of an oscillation in this particular case.

However, there have been reports from sources such as [4] which claim that "random input noise present in the ADC under test will cause the voltage excursion not to be a uniform oscillation waveform". Under this premise, they concluded that the oscillation period is not an accurate parameter to derive INL or DNL. On the other hand, the nature of this noise is not mentioned. If the noise is a zero-mean process for example, taking multiple repeated oscillation period measurements and taking the average will reduce the estimation error.

3. Analog Signal Generator Design

The signal generator consists of 2 current mirrors that have their currents controlled by switches. The switches open and close in order to charge and discharge a capacitor at the output node. The resulting output waveform resembles a triangle waveform. The magnitude of the current can be controlled by 2 control voltages. A graphical representation of the design is given in Figure 3.

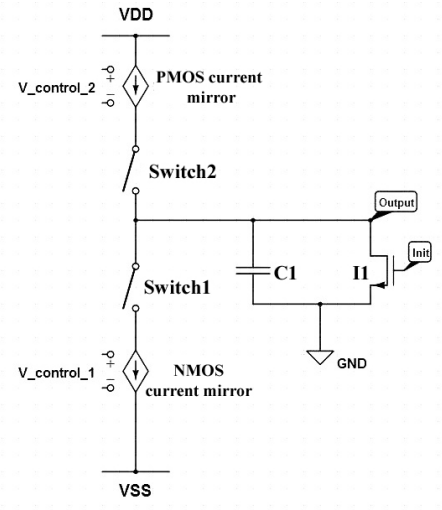

Figure 3: High level representation of the analog signal generator

In simulation these voltages were controlled manually in order to shift the DC operating point of the signal generator and control the oscillation amplitude as needed. However, in practice there needs to be precise control of these voltages in order to calibrate and operate the signal generator. This can be done with a calibration circuit that will be discussed later in this section. Table 1 lists some of the important specifications for the ADC and signal generator. Take note that the requirement for a low noise negative supply voltage implies that there is an added cost of a dedicated pin on the ATE.

Table 1: Supply voltage and output voltage specifications

Signal generator analog supply voltage	-1.3V – 3.3V
Signal generator output voltage range	0 – 2V
ADC analog supply voltage	0 -3.3V

3.1 Current mirror design and Schematic

The current mirror schematics are depicted in Figure 4 and Figure 5. Both current mirrors include control voltages which are meant to set the DC current in the current mirrors. Initially, the switch devices for the current sources were placed close to the output capacitor similar to the design presented in [5].

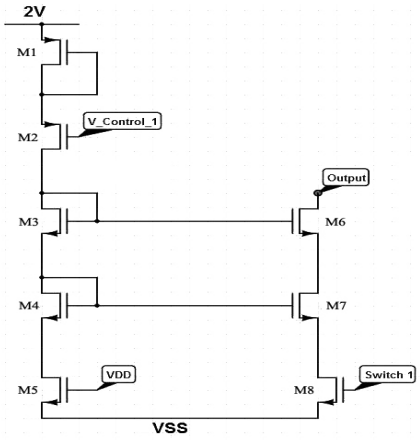

Figure 4: NMOS current mirror schematic

During switching, there is a significant amount of charge injection and clock feed through to the output capacitor which made controlling the oscillation amplitude dependent on the amount of charge injected as well as the current in the cascode branches. The charge injection effect is more significant as the capacitor size is decreased. The effect on the waveform manifests in the form of large non-linear voltage spikes near the peaks of the saw-tooth waveform when switching occurs. Having dummy switches near the capacitor helps to cancel some of the charge injection effects but not completely. Using complementary switches produced similar results to using dummy switches. Furthermore, the actual distribution of the injected charge in the actual fabricated devices in silicon is not very well understood and might be different than what was predicted in simulation.

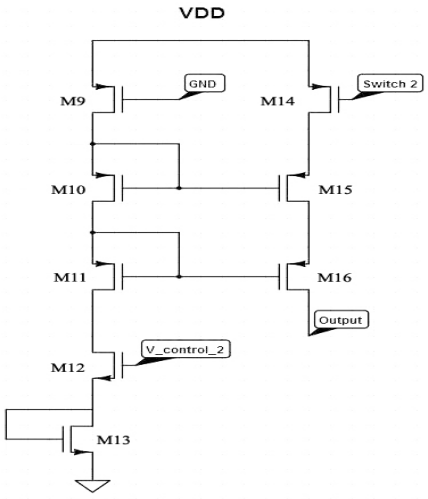

Figure 5: PMOS current mirror schematic

To solve this issue, the switches were placed closer to VDD and VSS. It is observed that the charge injection effect is reduced significantly due to the "shielding effect" the MOS cascodes provide to the capacitor node. By isolating the output capacitor from the switches, it is anticipated that charge injected during switching is not dumped onto the output capacitor. Instead, the short circuit path to AC ground is the preferred path for the electrons and holes during switching.

3.2 Proposed Calibration circuit

The purpose of a calibration circuit is to adjust the DC current magnitudes in the current mirrors as needed. Currently for simulation purposes, the control voltages in the signal generator are fixed voltage sources. However, it is possible to calibrate the control voltages internally through a feedback loop and a switched capacitor circuit approach that was presented in [2]. For OBIST, calibration is only meant to ensure that the current sources are similar and to ensure that the signal is able to oscillate periodically.

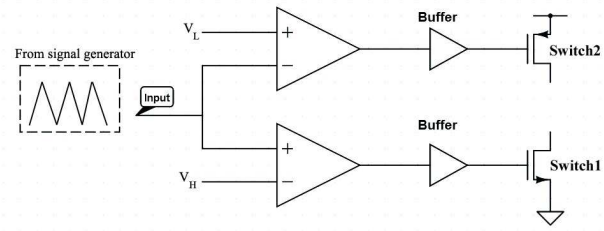

Figure 6: Oscillation block for calibration

The feedback mechanism consists of an oscillation block that would force the signal generator to oscillate between a predetermined voltage interval and a switched capacitor block that would adjust the control voltages in the current mirrors accordingly. An example of how the oscillation block might be implemented is given in Figure 6. The block consists of 2 comparators which measure whether the saw-tooth waveform from the current mirrors is above V_H or below V_L. Subsequently, that information is relayed to the control logic or directly to the MOS switches which forces the oscillation to be contained between V_H and V_L.

The resulting oscillation is then passed through an LCD block which will convert the saw-tooth waveform into a series of pulses as shown in Figure 7. The pulse width of the signal is a representation of the high-to-low and low-to-high transition periods. Based on this, the BIST Engine can tell whether the signal is periodic and whether the rise time and fall time of the analog input are similar when given a reference clock pulse. When a decision is made as to whether there needs to be more or less current in the current mirrors, the tuning of the control voltages is done by a switched capacitor block.

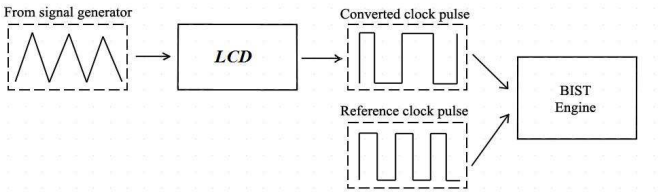

Figure 7: Using clock pulses to analyze the output from pre-calibrated signal generator

The switched capacitor circuit block acts like a high resolution cyclic DAC. It is the block that generates the control voltages and was previously used to calibrate the slope for adaptive linear ramps [3]. The circuit operates based on charge distribution between C1 and C2 where C1 is

charged to either V_{ref} or discharged to ground. Then, S1 is closed and the other switches are opened. When C1 and C2 reach equilibrium, some charge will be dumped onto C2 or moved from C2 to C1.

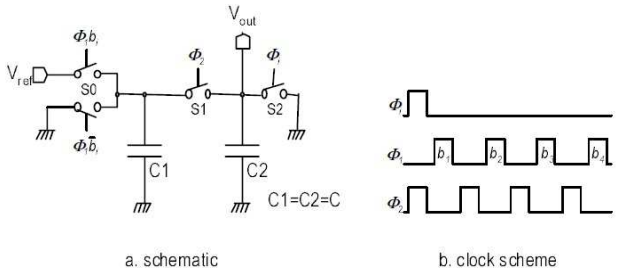

Figure 8: Switch capacitor circuit to generate control voltages for current mirror [2]

Based on the schematic presented in Figure 8, we can show that the circuit is able to increment or decrement the voltage at V_{OUT} by a small value provided C2 >> C1. With C2 at some initial value, V_i and C1 pre-charged to V_{ref}, it can be shown that the final voltage, V_f is given by equation (3) with the ratio of C1 to C2 being a small value. Conversely, if C1 is grounded beforehand, then the final voltage is given by equation (4) where the initial voltage is reduced by some small fraction.

$$V_f = V_i + \frac{C1}{C2} V_{ref} \quad (3)$$

$$V_f = V_i \frac{C2}{C1 + C2} \quad (4)$$

4. BIST Engine Design

The designed proposed in this paper utilizes a timer based concept to estimate the code width. The design is intended to be small and easy to implement. Figure 9 shows a high level overview of the proposed OBIST system together with the analog input generator block.

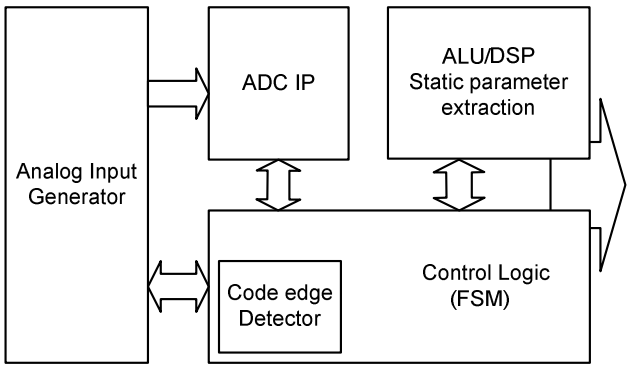

Figure 9: High Level block diagram of OBIST system

There are 2 modes of operation which are normal mode and diagnostic mode. In normal mode, the BIST will indicate the upper and lower bounds of the static parameter it is measuring at the end of the test. Unlike histogram testing where a large amount of output codes from the ADC has to be stored prior to processing, OBIST has the advantage of being able to estimate individual code widths in a serial fashion. For example, in a 10-bit ADC, there are 1024 possible output codes and a DNL test could start by estimating the 1 → 2 transition code width and end with the 1021 → 1022 code width estimation. The overall DNL is represented by the code width that has the highest DNL during the test. Hence, there is more flexibility in terms of the ability to discard the majority of the DNL estimations during the BIST test. There is also no need to store any of the raw ADC output codes in on-chip memory. Diagnostic mode assists the user in debugging for purposes such as failure analysis. There are three main components of the BIST that will be addressed in this section.

- Control Logic (CL)
- Code Edge Detection
- Static Parameter Extraction

4.1 Control Logic

The Control Logic (CL) is a system that coordinates the BIST for performing tasks such as calibration and initiating the analog input signal generation. The CL contains a finite state machine (FSM) that controls the ADC, analog signal generator circuit, calibration circuit, parametric extraction block and code detector block. The CL has full control over the BIST after an initial "BIST enable" signal is asserted.

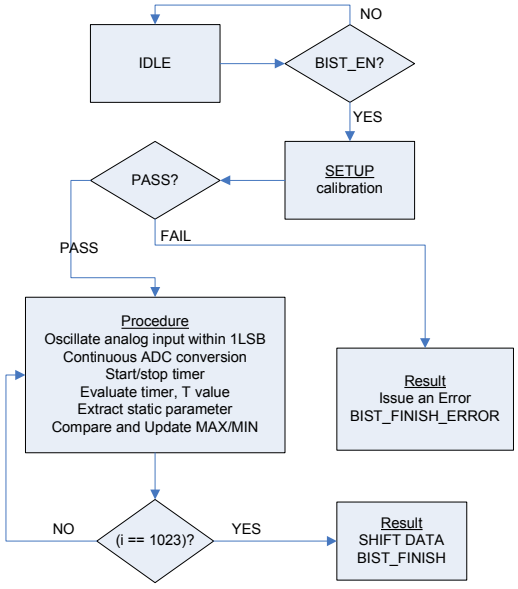

Figure 10: OBIST test procedure flow chart

After BIST_EN is asserted, the analog input generator and ADC have to be powered up. During the power up sequence, the analog input generator is calibrated while the ADC will be programmed to continuously sample and convert the analog inputs to its digital equivalent value. The code edge detector is triggered by the ADC_DONE signal that indicates when the conversion is done and DOUT [9:0] is valid. Once ADC_DONE is high, the code edge detector will

read and compare the output with an expected output code. The code detector enables the CL to decide when to ramp up or ramp down the input stimulus. Figure 10 shows the OBIST test procedure flow chart.

The input signal will oscillate for a predetermined number of cycles between two adjacent output codes that is controlled by the CL. Next, the CL forces the signal generator to oscillate between the next pair of output codes. This sequence is repeated until all output codes have been covered. The number of oscillation cycles to run per code bin can be controlled accordingly to reduce test time if desired.

4.2 Code Edge Detector

This block serves as a mechanism to detect the changes in the ADC output and relay that information to the control logic. When the analog signal reaches point 2 from point 1 as shown in Figure 11, the ADC output will change to another output code, i+1. The Code detector will trigger a signal that goes to a timer when the output code jumps from current code, i to i+1 or i-1.

To summarize, when code edge detector is triggered:

1. A 'timer' will either start or stop. The timer is used to track time taken for the input signal to sweep across the code width.
2. Control logic will force analog input generator to ramp up or ramp down analog signal accordingly.

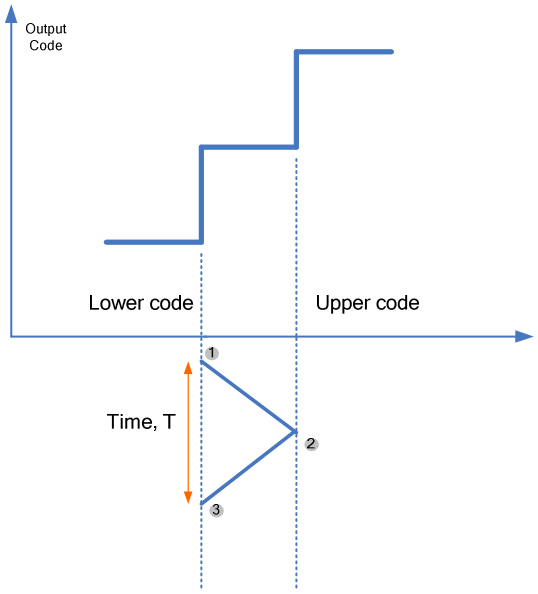

Figure 11: Measuring the code width of an ADC using a timer

The timer measures the time it takes to go from point 1 to point 3. The timer value, T, corresponds to the code width measured. In order to gain better precision, the timer should be clocked with frequency higher than ADC's sampling frequency. In contrast to the OBIST method presented in [1] that attempts to indirectly measure the oscillation frequency of the signal generator with a FNC block, this approach attempts to measure the code width. The condition that is required for this method to work is that the analog input signal has to be periodic. This is due to the fact that the timer does not compensate for frequency shifts as the DC operating level is adjusted to cover all codes. The oscillation continues for a set number of cycles until the BIST captures a few measurements for T. The average value for T is taken to average out any small random fluctuations in periodicity that may be present.

4.3 Static Parameter Extraction

The parameter extraction block is supposed to process the timer data from the code width measurements to produce an estimate on ADC static parameters such as INL and DNL. The block consists of an Arithmetic Logic Unit (ALU) and memory. The purpose of the ALU is to execute certain operations like addition, subtraction, multiplication and division. The ALU complexity versus the accuracy of the computations should be considered to optimize the number of gates needed to design an ALU which satisfies the computation and timing requirements.

Upon transition to new code bin, the code edge detector will forward the contents of timer register into this block. The static ADC parameters are extracted though several arithmetic operations. These operations will occur concurrently with the BIST. The CL block checks if the static parameter extraction block is idle before any attempt to extract parameters for each code bin is executed.

4.3.1 Differential Non-linearity (DNL)

DNL is defined as the difference between the measured code width and the ideal code width.

$$DNL(i) = K\left(\frac{T(i)}{T_{ideal}} - 1\right) \qquad (5)$$

The term enclosed in brackets in equation (5) represents the relative deviation of the timer value from the ideal. This deviation is correlated to the actual DNL value by a constant factor K that is determined either through experimental testing or simulations.

The timer value T, is a numerical representation of the relative size of the code width. In equation (5), T(i) is the time taken for the input signal to complete one oscillation. T_{ideal} is the ideal timer value when 1 oscillation is completed with a 1 LSB amplitude. The ideal timer value on the actual design implementation would vary as a function of the analog input oscillation frequency when it is oscillating with amplitude of 1 LSB and the clock speed of a timer. This value can either be pre-determined during simulations or calculated during the calibration phase.

4.3.2 Integral Non-linearity (INL)

INL is usually defined as the maximum deviation of the ADC transfer function from the ideal transfer function after

subtracting off the offset error but this approach is not suitable for OBIST since there is no way to determine the offset error accurately. There are also instances where INL is expressed as a running sum of DNL errors as shown in equation (6) and this is the same approach applied when the BIST system attempts to estimate the ADC INL. There is an inherent problem with this definition which lies in the amount of uncertainty in each of the calculations. Each estimate of DNL(j) contains some unknown uncertainty to the estimate. As we sum up the DNL values, these uncertainties sum up as well.

$$INL(i) = \sum_{j=1}^{i} DNL(j) \qquad (6)$$

More recent advancements in ADC testing algorithms have introduced BIST systems that operate using Stimulus Error Identification and Removal (SEIR) based linearity testing in order to estimate INL [6],[7]. The algorithm ensures the uncertainty in INL is bounded by a known value but increases the memory and ALU requirements significantly. Whether it would be necessary to integrate SEIR testing into OBIST at the cost of significantly more hardware overhead is still uncertain until more empirical data on the error bound for the INL estimates in OBIST is obtained. At the very least, it offers a feasible alternative to estimate INL if (6) does not produce sufficiently accurate results.

5. Simulation Results and Discussion

5.1 Analog signal generator

The signal generator showed in simulation that it is capable of having a voltage swing of as small as 2mV which corresponds to 1 LSB for a 10-bit ADC with a 2V input voltage range. The oscillation frequency was at 625 kHz. However, to achieve this goal, we needed to use a 150pF capacitor. The waveform for the oscillation is shown in Figure 12. Such a large capacitor cannot be practically made in integrated circuits without incurring a large chip area overhead. Having smaller capacitors on the other hand would cause higher oscillation frequencies and would require the ADC to have a much higher sampling rate in order to avoid overshoot. Overshoot is the state where the input signal slew rate is too high for the ADC to detect a code transition resulting in the test falsely diagnosing the ADC to have "missing codes". A possible solution for lowering the oscillation frequency of the signal generator is to place an external capacitance on the Device-Under-Test (DUT) board instead. This external capacitance is connected to the output of the signal generator and is placed as close as possible to the chip. It is important to ensure that the noise on the ground of the capacitor is low because the oscillation amplitude of the BIST is small. This means that if the ATE common ground is too noisy, there needs to be proper shielding provided.

Efforts to reduce the current in the cascode branches instead of having to deal with large capacitances result in transistors having to operate very close to triode region or in triode region. The issue of overshoot can also potentially arise from the non-linear behavior at switching points where there is a spike of current during switching that causes voltage spikes at the output node with very high slew rates. These voltage spikes, as seen in Figure 12, become more pronounced as the capacitor size decreases.

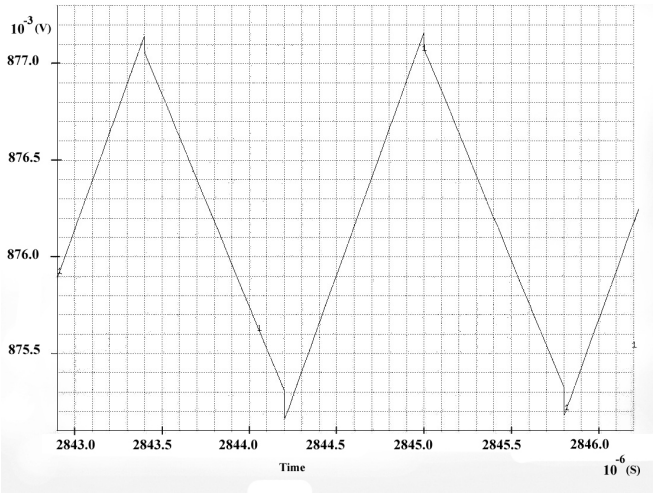

Figure 12: Oscillation within a 2mV range at 625kHz using a 150pF capacitor

A rough approximation of the oscillation frequency of the signal generator is shown in equation (7) which was taken from [1]. This equation assumes that both mirrors have the same current magnitude. The ADC oscillation frequency is a function of the output capacitance of the signal generator, the currents of the two current sources and the ADC conversion time, t_C. V_{Tk}^A and V_{Tj}^A are 2 adjacent output code transition voltages.

$$f_{OSC} = \frac{1}{\left(\frac{2(V_{Tk}^A - V_{Tj}^A)C}{I} + 4\,t_C \right)} \qquad (7)$$

It is interesting to note that the term $\frac{C}{I}$ in equation (7) can be thought of as the inverse of the slew rate of the signal generator. Given that the transition voltage levels of an ADC are ideal, the oscillation frequency of the signal generator is not constant if channel length modulation is not neglected in the signal generator. The effect is deemed tolerable in the research presented in [1] for DNL calculations. However, the effect of channel length modulation is more pronounced in deep submicron transistors which cause the output current to vary with the DC output operating point of the signal generator which directly introduces errors in the slew rate. Slew rate variance is an issue because it introduces errors into the oscillation frequency which directly impacts the measurement of DNL. Table 2 below summarizes the effects of DC output level on the oscillation frequency of the signal generator.

The data for Table 2 was collected by first calibrating the signal generator at a certain DC operating point where the

signal generator is oscillating with amplitude of approximately 2mV with an initial oscillation frequency of 4 MHz. This is done by adjusting the control voltages until the initial conditions are met. The DC operating point was then shifted by forcing the signal generator to oscillate near the extremities of the ADC analog input range. The idea is to keep the oscillation amplitude similar and vary the oscillation frequency or the control signal pulse width as needed. In this case, the ADC under test has an analog range of 0V to 2V for a load capacitor of 150pF.

Table 2: Effects of calibrating the signal generator at different DC operating points

Scenario 1: Calibration near 0V		
Calibrated DC voltage level (V)		0.002371
Calibrated oscillation frequency (MHz)		4.00
Calibrated oscillation amplitude (mV)		1.997
Shifted DC voltage level (V)		1.997
Measured oscillation amplitude (mV)		1.997
Measured oscillation frequency (MHz)		3.4965
Frequency deviation (%)		-12.59
Scenario 2: Calibration near 2V		
Calibrated DC voltage level (V)		1.998
Calibrated oscillation frequency (MHz)		4.00
Calibrated oscillation amplitude (mV)		2.016
Shifted DC voltage level (V)		0.002367
Measured oscillation amplitude (mV)		1.973
Measured oscillation frequency (MHz)		3.4364
Frequency deviation (%)		-14.09
Scenario 3: Calibration near 1V		
Calibrated DC voltage level (V)		0.9896
Calibrated oscillation frequency (MHz)		4.00
Calibrated oscillation amplitude (mV)		2.05
Shifted DC voltage level (V)	1.997	0.007196
Measured oscillation amplitude (mV)	2.041	2.067
Measured oscillation frequency (MHz)	4.00	4.00
Frequency deviation (%)	-	-

The simulations for scenario 3 imply that the frequency variation is small if the device is calibrated at a voltage close to 1V. The signal generator was able to operate at the chosen DC levels without the need to change the oscillation frequency. In this case, adjusting the pulse width of the control signals was sufficient without needing to change the oscillation frequency. Scenario 1 and scenario 2 suggest that calibrating the signal generator at the extreme ends of the analog input scale can introduce oscillation frequency error of at least 14% or more. Hence, it appears that the effect of channel length modulation can be minimized if the calibration point is at the midway point of the ADC analog input range.

A common approach to counter this frequency deviation phenomenon is to increase output impedance by increasing the device length of the MOS transistors. Increasing channel length while keeping the drain currents constant has limits because of the constraints in transistor dimensions imposed by the foundry. For example, increasing transistor length would require either higher overdrive voltages or higher width to keep drain currents constant but devices cannot exceed a certain width. Increasing overdrive voltages on the other hand limits the output swing of the signal generator.

As for the significance of the noise produced by the circuit, the thermal noise produced from charging the capacitor is dependent on the size of the capacitor used and is given by equation (8) where 'T' is the absolute temperature and 'k' is the Boltzmann constant.

$$V_{noise,rms} = \sqrt{\frac{kT}{C}} \qquad (8)$$

For example, a 150pF capacitor load at a nominal operating temperature of 55 degree Celsius yields about a 5.49 μ Vrms of noise at the output node. This suggests that thermal noise might not be a very significant issue during testing since the Signal-to-noise Ratio (SNR) is approximately 51dB when using 2mV oscillation amplitude. The 10-bit ADC under test has been shown to have similar SNR values in the low 50dB range during characterization tests.

6. Conclusion

OBIST may still be useful for characterizing static parameters such as DNL on ADCs despite device processes scaling down to smaller nodes. For this particular work, we considered an ADC with 10 bits of resolution and a 0 – 2V analog input range. Initial findings suggest that the method may be more suited for applications in low resolution - high speed ADCs. It has been shown in simulation that testing 10-bit ADCs is still feasible. The design presented also outlines a possible implementation of a calibration circuit by adapting a switched-capacitor circuit originally meant for ramp testing of ADCs. In addition, this work also introduces the idea of a timer based measurement scheme instead of the traditional frequency based measurement scheme.

Acknowledgment

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