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Passive and active optical bit-pattern recognition structures for multiwavelength optical packet switching networks

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Abstract: Next generation High-Speed optical packet switching networks require components capable of recognising the optical header to enable on-the-fly accurate switching of incoming data packets to their destinations. This paper experimentally demonstrates a comparison between two different optical header recognition structures; A passive structure based on the use of Fiber Bragg Gratings (FBGs), whereas the active structure employs Opto-VLSI processors that synthesise dynamic wavelength profile through digital phase holograms. The structures are experimentally demonstrated at 10Gbps. Performance comparison between the two structures is also discussed. These optical header recognition structures are attractive for multiwavelength optical network and applications.

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OCIS codes: (070.4550) Optical correlators; (070.5010) Pattern recognition; (090.1970) Diffractive optics; (060.2330) Fiber optics communications

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1. Introduction

The demand for an effective technique to recognise optical packet headers on the fly without any optical-to-electrical conversion have been increased. A promising technique for recognizing optical packet headers on the fly involves the use of time-domain optical correlators to correlate an incoming header pattern with predetermined bit patterns of a look-up table [1, 2]. Each correlator is configured to match a specific header pattern that is assigned to a destination port. An autocorrelation function of a very high peak is generated whenever the optical header bit pattern matches a pattern of the look-up-table, while for other patterns, only low intensity cross-correlation functions are produced.

On the other hand, the performance of optical packet-switched networks relies heavily on the methods used for encoding, transmitting, and extracting the optical header [3]. Headers and payloads can be transmitted on the same wavelength [3], [4], or on different wavelengths [3], [5]. Also, the payload can be delivered at a designated wavelength while the header is transmitted on multiple wavelengths [6]–[13]. An asynchronous optical packet switched network based on combining wavelength and time for header generation has been reported [13, 14], where payloads is carried on a wavelength while the header is coded on multi-wavelength carrier. Employing multiwavelength header patterns enables the node to quickly and efficiently process the header, and easily differentiate it from the payload and extract it from the packet.

Recently, several schemes for realising multi-wavelength header correlators have been proposed, which are based on fiber Bragg gratings (FBGs) [6]–[8], semiconductor optical amplifier (SOA) [9], [10] and serial-to-parallel conversion [11], [12].

In this paper, a comparison study of two attractive multiwavelength optical header recognition structures. The first structure utilizes passive arrays of FBG to construct a bank of correlators, while the second structure employs a single Opto-VLSI processor [15] to construct the correlators, thus allowing dynamic optical header recognition. The recognition of 4 bit pattern at 10Gb/s carried out for both structures is experimentally demonstrated.

2. FBG and OPTO-VLSI processor

Fiber Bragg gratings (FBGs) and Opto-VLSI processors are the key components for the passive and active multiwavelength optical header recognition structures reported in this paper. The use of Wavelength Division Multiplexing (WDM) provides a new dimension for solving capacity and flexibility problems in optical networks, and these features allow for

novel optical header recognition structures to be realised, thus offering much more flexibility than their current counterparts.

A fiber Bragg grating (periodic perturbation of the refractive index along an optical fiber length) is one of the most important optical component that revolutionarized WDM systems, because of its high noise immunity, low manufacturing cost linearity, compact size, and ability to process signal in both reflection and transmission [16], [17].

By injecting a spectrally broadband source of light into an FBG, a narrowband spectral component centred at the Bragg wavelength of the FBG is reflected while the other spectral components are transmitted with negligible attenuation.

On the other hand, Opto-VLSI processors are reconfigurable optical signal processors capable of dynamically steering, splitting or demultiplexing optical signals. An Opto-VLSI processor comprises an array of liquid crystal (LC) cells driven by a Very-Large-Scale-Integrated (VLSI) circuit that generates digital holographic diffraction gratings to steer and/or shape optical beams [18] as shown in Fig. 1. Each pixel is assigned a few memory elements that store a digital value, and a multiplexer that selects one of the input voltages and applies it to the aluminum mirror plate. An Opto-VLSI processor is electronically controlled, software-configured, polarization independent, cost effective because of the high-volume manufacturing capability of VLSI chips as well as the capability of controlling multiple optical beams simultaneously, and very reliable since beam steering is achieved with no mechanically moving parts [19]. These attractive features have opened the way for the Opto-VLSI technology to be employed in reconfigurable optical networks [18-21]. Figure 1 also shows a pixel block loaded with a phase hologram which acts as a blazed grating that steers an optical beam incident on that pixel block. More information about the capabilities of Opto-VLSI processors can be found in [15], [18-21].

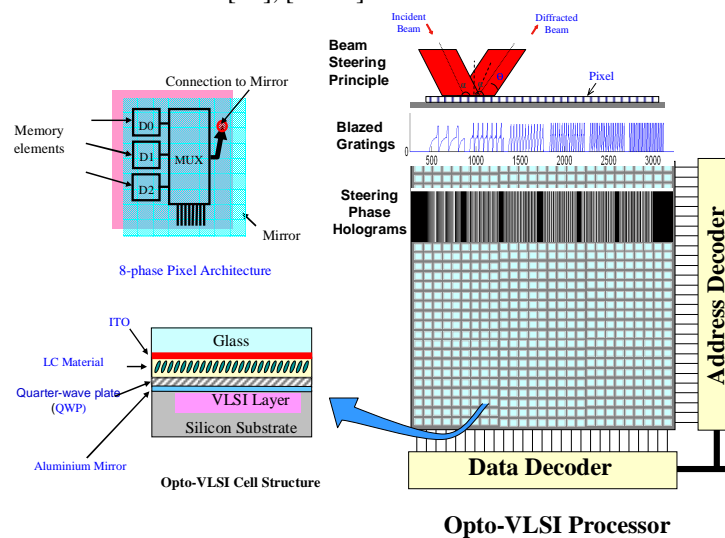


Fig. 1. Opto-VLSI processor structure and illustration of optical beam steering.

3. Multiwavelength header recognition structures

In a multi-wavelength header network, the payload is transmitted on a wavelength λ_0 , whereas the header pattern modulates wavelength division multiplexed optical carriers ($\lambda_1, \lambda_2, \dots, \lambda_N$). When the packet arrives at the routing node, a small portion of the incoming packet is routed to a bank of correlators, each configured with a different wavelength profile that can recognise a specific header bit pattern. Figure 2 shows a node of a packet switched optical network, with the optical correlator banks can either be passive based on the FGB structure (left) or active based on the Opto-VLSI structure (right).

For the passive structure, arrays of FBGs of different Bragg wavelengths placed at a spacing that corresponds to half the header bit time. Each FBG array is designed with a different wavelength profile that matches a specific header bit pattern. The wavelength profile is realised by using 100% reflectivity gratings and 0% reflectivity gratings, which correspond to “1” and “0” bits, respectively. The reflected wavelengths of each FBG array are detected by a photodetector followed by a simple decision electronic circuitry that compares the peak of the detected signal to a threshold level. Upon detection of a high-peak autocorrelation function, the optical switch at the node is driven to route the optical packet to the appropriate destination.

On the other hand, the active structure employs an Opto-VLSI processor that generates the routing look-up table through spectral masking of the header wavelengths with digital phase holograms, thus synthesising dynamic wavelength profiles. The active window of the Opto-VLSI processor is logically partitioned into rows of pixel blocks, where each pixel block representing different wavelength, driven by a digital phase hologram. An autocorrelation function is generated when the header wavelengths matches the wavelength profile. Upon reflection off the Bragg gratings, the WDM components of the header are equally split horizontally, collimated, and then the WDM channels are spatially demultiplexed, by a grating plate, along different directions and mapped onto N pixel blocks on the 2-dimensional Opto-VLSI processor, whose active window is logically partitioned into rows of pixel blocks. A wavelength component incident on a pixel block can either be steered along a specific optical path thus coupled, through another grating plate, which multiplexes the WDM channels, into the output fiber collimator, or deliberately steered “off-track” so that its power is not coupled back into the fiber collimator. By loading the pixel blocks with optimized digital phase holograms, the intensities of the different wavelengths reflected off the pixel blocks of a row can be arbitrarily attenuated to realise a wavelength profile that matches a specific header pattern. Since the wavelengths had been delayed by one bit time increments, an autocorrelation function exhibiting a high peak at its centre of symmetry is detected by the photodetector when the header bit-pattern matches the wavelength profile generated by the Opto-VLSI processor. By comparing the photodetected signal to a threshold level, an electrical signal is generated, which drives the switch to route the individual optical packet. Otherwise, if the header bit-pattern does not match the wavelength profile, the correlator output exhibits no spike (cross-correlation) and hence the header pattern is not recognised by the threshold detector.

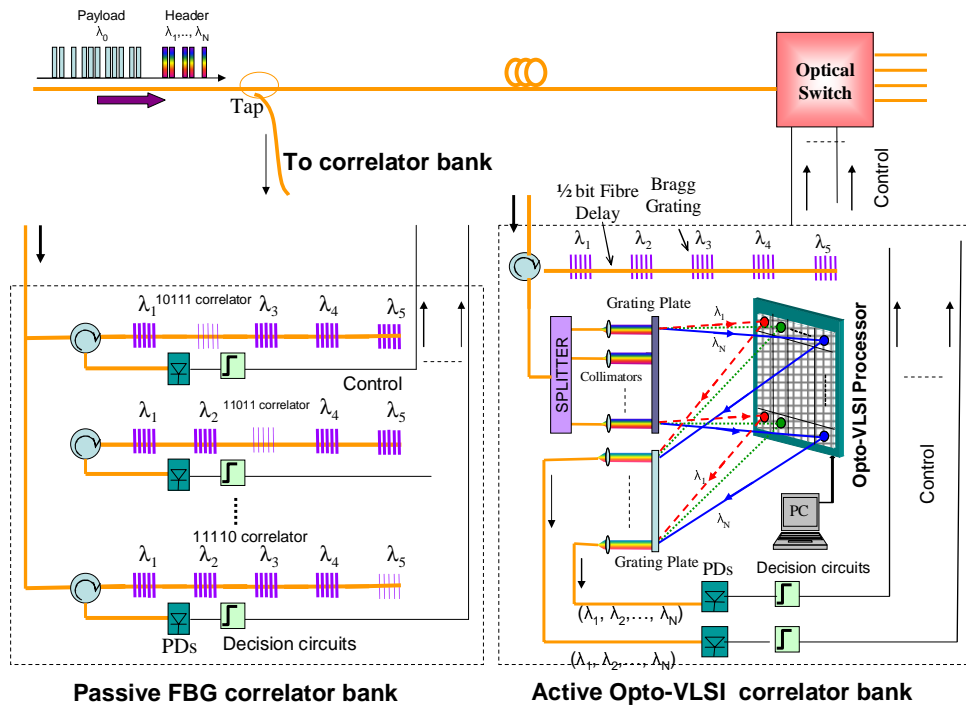


Fig. 2. Multiwavelength node structures using FBG arrays and Opto-VLSI processor to construct the correlator bank.

4. Experiment setup and results

Two experimental setups were carried out to demonstrate the performance of the correlator structures, as discussed below.

4.1 Demonstration of the passive FBG-based optical header recognition structure

A 4-bit optical correlator demonstrator was set up, as shown in Fig. 3. A pattern generator was used to generate a 4-bit packet 1011 at 10Gbit/s. A low coherence Amplified Spontaneous Emission (ASE) source was launched into an electro-optic modulator (EOM). The modulated light was equally split and routed into two arrays of four FBGs configured with different wavelength profile. The first FBG array has a wavelength profile that matches the input bit pattern 1011, while the second FBG array has a “no-match” with a wavelength profile of 1101. The first FBG array had 10mm center-to-center spacing between the FBGs whose reflectivities were 100% at 1551.6 nm, 1554.5 nm, and 1556.1nm and 0% at 1553nm, The second FBG has the same center-to-center spacing but the reflectivities were 100% at 1551.6 nm, 1553nm, and 1556.1nm and 0% at 1554.5nm. The three reflected wavelengths of each correlator were detected using a high speed photodetector and monitored by a high-speed digital oscilloscope.

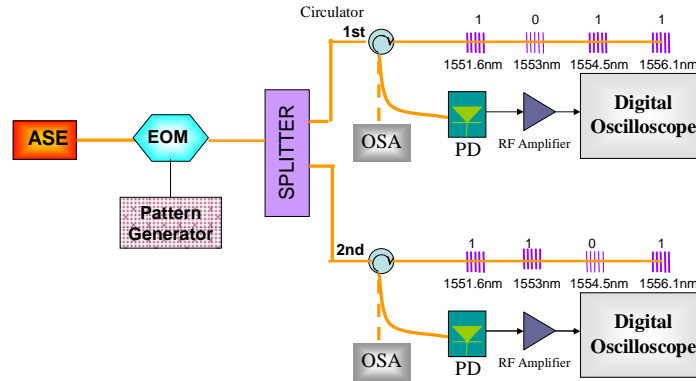


Fig. 3. Experimental setup for the multi-wavelength bit-pattern recognition

Figure 4(a) shows the wavelength spectrum reflected off the first FBG array, where the 1553 nm wavelength was not reflected back, thus, a wavelength profile (1011) was generated that matches the input bit pattern. As a result, the measured detected signal was an autocorrelation function exhibiting a high peak at its centre of symmetry, as shown in Fig. 15(a). Since the autocorrelation function exhibits a high peak at its centre of symmetry, the correlation output can be compared to a threshold level, and a simple decision electronic circuitry (not shown in Fig. 3) can be used to drive the switch to route the individual optical packet.

Figure 4(b) shows the wavelength spectrum reflected of the second FBG, which generates a wavelength profile that does not match the input bit pattern. As a result, the detected signal has no high peak at its centre of symmetry (cross-correlation) as shown in Fig. 5(b).

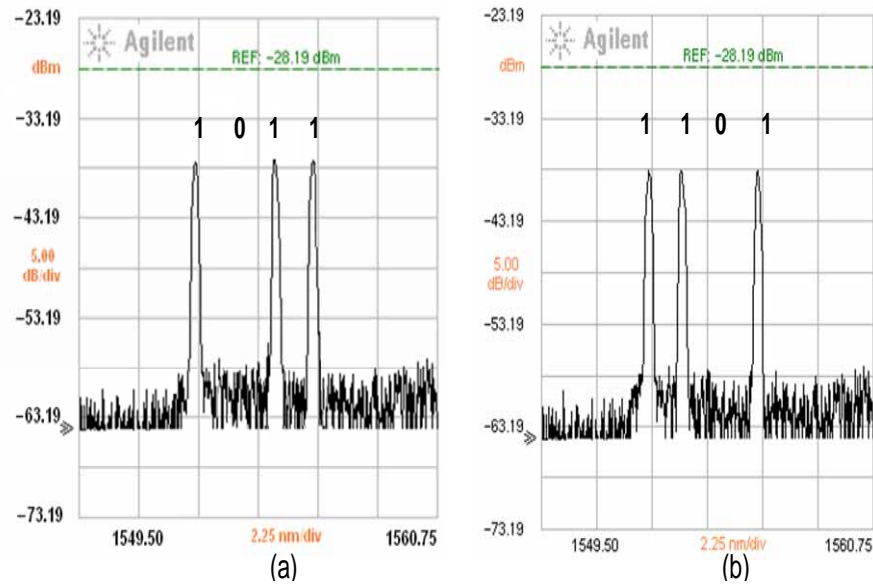


Fig. 4. (a) Wavelengths reflected off the first FBG with a wavelength profile matches 1011 bit pattern. (b) Wavelength profile reflected off the second FBG mismatching 1011 bit pattern.

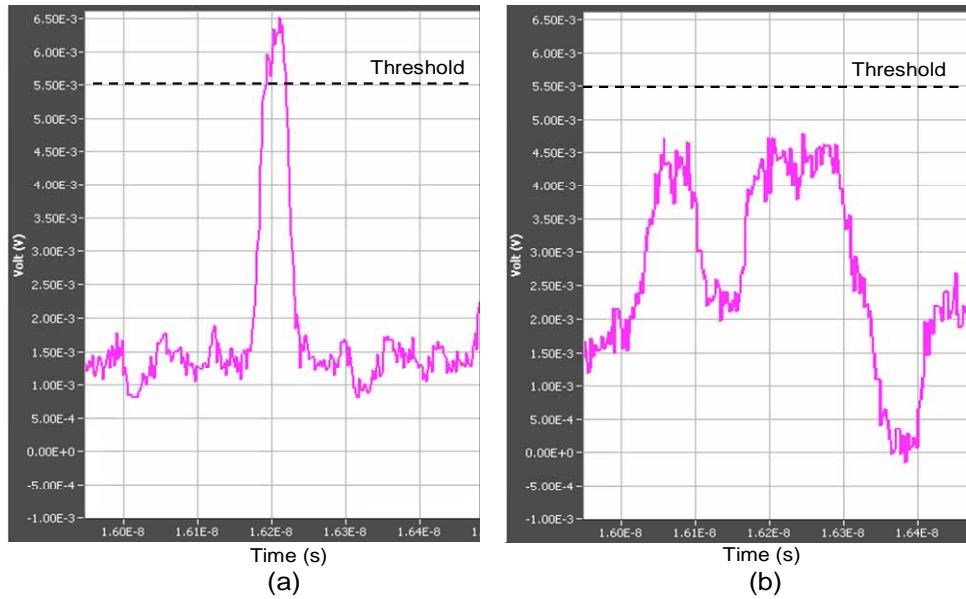


Fig. 5. Measured output waveform (a) when the wavelength profile matches the input bit pattern 1011 (autocorrelation). (b) When the wavelength profile does not match the input bit pattern 1011 (cross-correlation).

We also investigated the case where the input bit pattern was changed from 1011 to 1101. In this scenario, the measured output of the first correlator is shown in Fig. 6(a), and the measured waveform of the second correlator is shown in Fig. 6 (b).

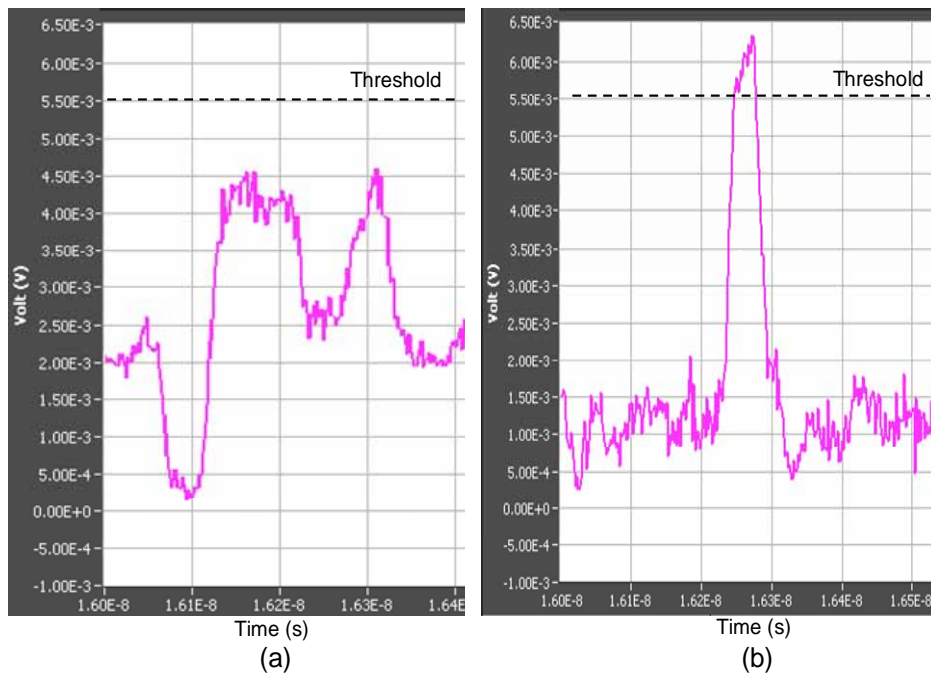


Fig. 6. Measured output waveform (a) When the wavelengths profile does not match the input bit pattern 1101 (cross-correlation). (b) When the wavelengths profile matches the input bit pattern 1101 (autocorrelation).

From the previous results, it is obvious that when the input bit pattern does not match the wavelength profile of the FBG array, the correlator output exhibits no spike and hence the bit pattern cannot be recognised by the threshold detector. This demonstrates the principle of the FBG optical correlator for multiwavelength bit pattern recognition.

4.2 Demonstration of the active Opto-VLSI-based optical header recognition structure

A 4-bit correlator demonstrator was set up as shown in Fig. 7. A low coherence Amplified Spontaneous Emission (ASE) source was launched into an electro-optic modulator (EOM) and intensity-modulated with a 10Gb/s bit pattern. The modulated light was launched into an optical fiber having an array of four fiber Bragg gratings equally spaced, with centre-to-centre at 10 mm. All FBGs had identical reflectivities of 100% and Bragg wavelengths of $\lambda_1=1551.6\text{nm}$, $\lambda_2=1553\text{nm}$, $\lambda_3=1554.5\text{nm}$, $\lambda_4=1556.1\text{nm}$, respectively.

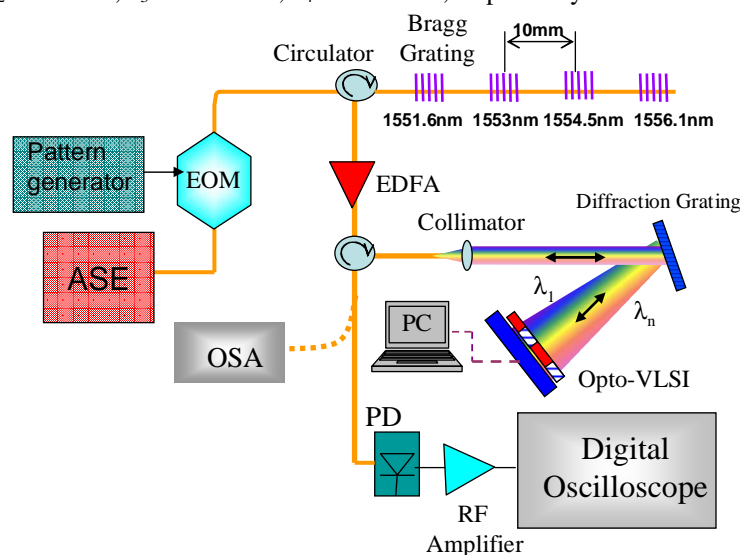


Fig. 7. Experiment setup for bit pattern recognition using an Opto-VLSI processor.

The FBG array spectrally sliced the incoming broadband optical signal into four different wavelengths, with an equal delay increment of one bit-time (corresponding to the round-trip propagation between two Bragg gratings).

The delayed multiple wavelengths reflected off the Bragg gratings were routed through an optical circulator and amplified using an erbium-doped fiber amplifier (EDFA). The wavelengths were then routed (by the second circulator) to a 1-mm diameter collimator and the collimated beam was launched towards a blazed grating of 1200 lines/mm grating surface. The latter spread the wavelengths along different direction and mapped them onto the active window of the Opto-VLSI that was logically partitioned into several pixel blocks that appropriately attenuated the different wavelength components to generate a wavelength profile that matches the bit pattern.

The Opto-VLSI processor used in the experiments had 1×4096 pixels. 256-level phase holograms were generated by applying appropriate voltage levels between 0V and 2 V to the individual pixels. A program was written in MATLABTM to generate and send command voltages in the form of image to the Opto-VLSI processor to generate optimized steering holograms for the incident wavebands. The program allowed the user to steer many input channels, each independently controlled in terms of position, width and phase profile. The initial phase hologram used for the real-time optimization procedure was a blazed grating.

Each wavelength band was allocated a pixel block that was independently addressed to reflect that band back along its incident optical path, hence coupling it into the fiber collimator with minimum attenuation, or to appropriately steer it away so its power is not coupled back into the fiber collimator, leading to independently-controlled optical attenuation for each wavelength band. The coupled-back optical signal was detected by a high-speed photodetector, and the detected waveform was displayed on a high-speed oscilloscope.

An Anritsu pattern generator was used to generate a 4-bit packet 1011 at 10Gbit/s, and the Opto-VLSI processor was loaded with proper wavelength profile which matches the input bit-pattern. Figure 8(a) shows the steering digital phase hologram, which coupled the wavelength components λ_1 , λ_3 , and λ_4 , and steered away the other wavelength component λ_2 , thus generating a wavelength profile 1011. Figure 8(b) shows the generated wavelength profile. The coupled-back optical signal was detected by the high-speed photodetector and the waveform was monitored using a high-speed digital oscilloscope.

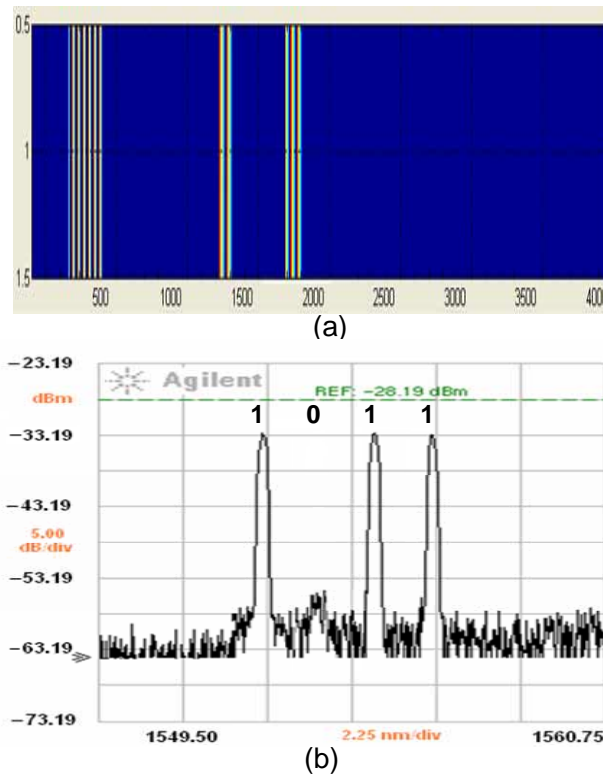


Fig. 8. (a). Digital Phase hologram loaded on the Opto-VLSI processor to generate 1011 wavelength profile, (b) wavelength profile that matches the optical bit pattern 1011.

Figure 9(a) shows the measured photodetected waveform, which corresponds to an autocorrelation with a high peak at the centre, resulting from the matching between the wavelength profile and the bit pattern.

When the input pattern was changed to 1101 and the wavelength profile was left without change the bit pattern mismatched the wavelength profile and a cross-correlation was generated as shown in Fig. 9(b). In this particular case, the correlator output exhibited no spike and hence the bit-pattern could not be recognised by a threshold detector.

However, when the Opto-VLSI processor was loaded with the proper digital phase hologram that matches the input bit pattern 1101, an autocorrelation was generated. Fig. 10(a)

shows the digital phase hologram loaded to recognise 1101 bit pattern. Fig. 10(b) shows its correspondence wavelength profile, and the measured output waveform is shown in Fig. 10(c), demonstrating an autocorrelation function that exhibits a high peak whenever the bit pattern and wavelength profile are matched.

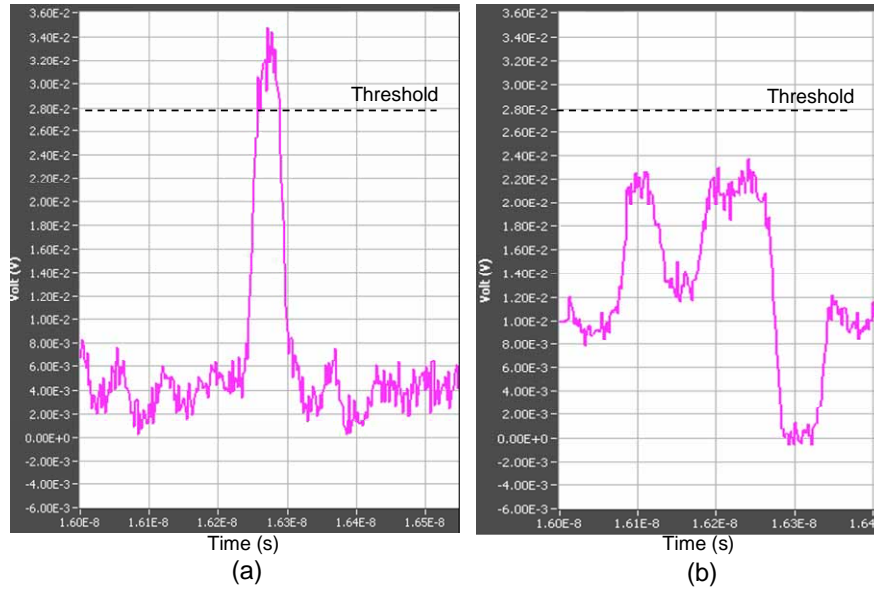


Fig. 9. Measured output waveform, (a) when the bit pattern matches the wavelength profile (autocorrelation). (b) When the bit pattern mismatches the wavelength profile (cross correlation).

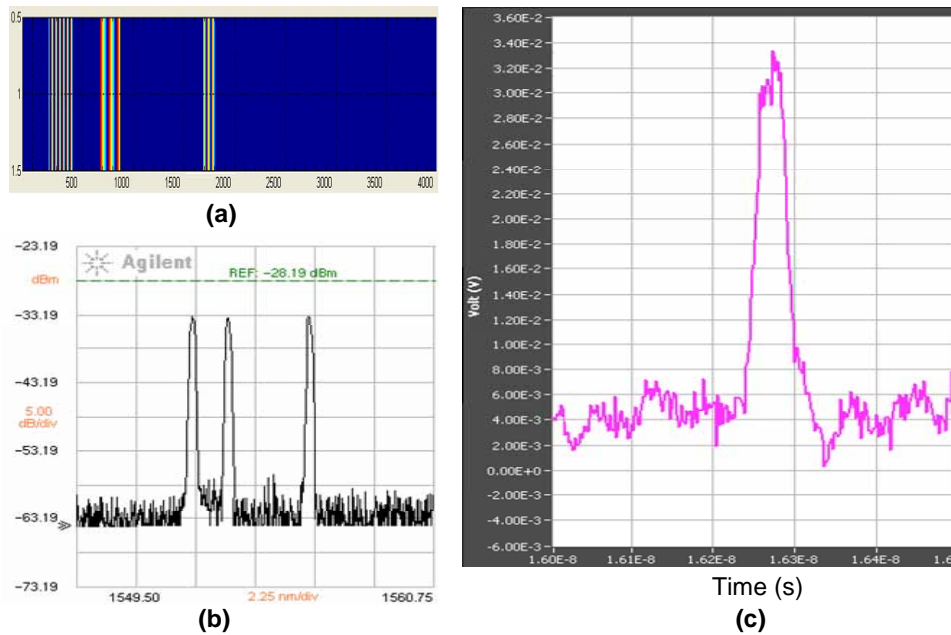


Fig. 10. (a). the loaded digital phase hologram to generate 1101 wavelength profile. (b). Wavelength profile that matches 1101 bit pattern. (c). The measured output waveform (autocorrelation)

5. Discussion

The results presented in this paper demonstrate the capability of the multiwavelength header recognition structures to recognise arbitrary bit patterns by generating an autocorrelation function whenever the wavelength profile matches the incoming bit pattern, or a cross correlation function otherwise. As a result, the use of multi-wavelength header transmission makes the correlator structures very attractive for ultra-high-speed optical networks.

In addition, it is important to note that when the correlator is configured to recognize a bit pattern, say 1011, and the incoming bit pattern is 1111, the photodetected output waveform produces a high peak that is above the threshold level, thus leading to a switching error. To uniquely recognize a pattern, an additional correlator configured in complement must be used in conjunction with an AND gate, as illustrated by Hauer et al. [2].

The main advantage using the FBG arrays in optical pattern recognition structures is the simplicity, low cost, and low insertion loss of FBGs. On the other hand, such passive structure requires N number of circulators, and it is not reconfigurable, leading service interruption whenever bit-rate or network upgrade is needed.

The advantage of using an Opto-VLSI processor is its unique reconfigurability feature that enables the synthesis of a dynamic look-up table of wavelength profiles that matches different header bit patterns. This capability enables future network expansion/upgrade to be performed without the need for service interruption. Unlike all other reported optical header recognition techniques that are designed for fixed data bit-rates, Opto-VLSI based optical correlators are transparent to the data bit-rate. Note that, for an optical header recognition structure, the optical switch architecture is simple and does not require a non-linear optical processing or synchronisation in the correlator for wavelength- and/or time-shifting of individual header bits. Note also that the optical power loss of the active Opto-VLSI correlator is 8-dB higher than that of the FBG passive correlator. This is due to the free-space-to-fiber coupling, and the insertion loss of the diffraction grating and the Opto-VLSI processor. However, this additional loss can be compensated for using an EDFA as shown in Fig. 7. Finally, the scalability of the active optical header recognition structure depends on the size of the active window and the bandwidth of the Opto-VLSI processor. The active window of the Opto-VLSI processor can practically be as large as 20mm×20mm. For a pixel size of 5 μ m×5 μ m, 4000×4000 pixel Opto-VLSI processors can practically be fabricated. Using pixel blocks of 64×64 pixels and a dead space of 64 pixels, headers of 32 bits can be realised. Moreover, Opto-VLSI processors have optical bandwidths exceeding 80 nm, thus the correlator architecture can be scaled 100 Gb/s and beyond.

6. Conclusion

Active and passive optical header recognition structures have experimentally been demonstrated at 10Gb/s. The non-reconfigurable passive structure has had header correlator banks constructed using arrays of fiber Bragg gratings, configured with predetermined wavelength profiles that match specific bit pattern at a fixed bit rate. The second structure has employed a single Opto-VLSI processor to construct the header lookup table of bit patterns that match wavelength profiles generated using digital phase holograms. Experimental results have shown that an autocorrelation function of a high peak is generated whenever the bit pattern matches the wavelength profile. Measured autocorrelation and cross-correlation waveforms of different bit pattern have demonstrated the capability of the passive and active structures to recognize specific and arbitrary bit patterns, respectively. It has been found that the optical power loss in the Opto-VLSI-based structure is higher than that of the FBG-based structure. However, the use of an EDFA has been shown to be effective in compensating for the high-insertion loss of Opto-VLSI processors.

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