2007

Opto-VLSI-Based reconfigurable free space optical interconnects architecture

Muhsen Aljada
Edith Cowan University

Kamal Alameh
Edith Cowan University

Yong Lee

I-S Chung

10.1117/12.696359

Opto-VLSI-based reconfigurable free-space optical interconnects architecture

Muhsen Aljada[a], Kamal E. Alameh[a], Yong-Tak Lee[b], Il-Sug Chung[b]
[a]Centre for MicroPhotonic Systems, Electron Science Research Institute,
Edith Cowan University, Joondalup, WA, 6027, Australia.
[b]Gwangju Institute of Science and Technology, Department of Information and Communication,
Gwangju 500-712, Korea.

ABSTRACT

This paper presents a short-distance reconfigurable high-speed optical interconnects architecture employing a Vertical Cavity Surface Emitting Laser (VCSEL) array, Opto-very-large-scale-integrated (Opto-VLSI) processors, and a photodetector (PD) array. The core component of the architecture is the Opto-VLSI processor which can be driven by digital phase steering and multicasting holograms that reconfigure the optical interconnects between the input and output ports. The optical interconnects architecture is experimentally demonstrated at 2.5 Gbps using high-speed 1×3 VCSEL array and 1×3 photoreceiver array in conjunction with two 1×4096 pixel Opto-VLSI processors. The minimisation of the crosstalk between the output ports is achieved by appropriately aligning the VCSEL and PD elements with respect to the Opto-VLSI processors and driving the latter with optimal steering phase holograms.

Keywords: Optical interconnects, Opto-VLSI processors, free-space communications.

1. INTRODUCTION

Optical interconnects are currently under intense investigation as potential high-speed data buses in electronic devices, multi-chip computers and signal processors [1]-[3], and it is anticipated that at the end of this decade optical interconnects will significantly reduce much of the board-to-board and processor-to-processor bandwidth burden in high-end computer systems [4]. Optical interconnects have been proposed for high-speed data communications in electronic computers and signal processors including polymer waveguides [5] [6], fibre image guides [7], [8], and fibre ribbons [4] [9], and free space optical interconnects using lens and mirror system [10]-[14].

Free-space optical interconnects are potential solutions to achieving high-bandwidth, low-power-consumption data communications. In addition, reconfigurability and multipoint interconnects are easier to realise with free-space optics, and much more processor arrays can be linked together [15], where the optical links are mainly achieved using VCSEL arrays for light emission attached on the top of a die and photodetector (PD) arrays integrated with high-speed drivers and receivers.

In this paper, we propose and demonstrate the concept of a dynamic reconfigurable optical interconnects architecture that can be used for chip-to-chip interconnection, parallel signal processing and computing. In this architecture, VCSEL and photodetector arrays are used to provide high-speed optical data link, in conjunction with two Opto-VLSI processors driven by digital phase holograms that reconfigure the switching states of the optical links.

2. OPTO-VLSI PROCESSOR

An Opto-VLSI processor consists of an array of liquid crystal (LC) cells driven by a Very-Large-Scale-Integrated (VLSI) circuit that induces digital holographic diffraction gratings to steer and/or shape optical beams [16], [17], as

shown in Fig. 1. Every pixel is assigned a few memory elements and a multiplexer that enable many input voltages to be applied to the aluminum mirror plate. An Opto-VLSI processor is electronically controlled, software-configured, polarization independent, cost effective, and very reliable since beam steering is achieved with no mechanically moving parts [17]. These attractive features open the way for the Opto-VLSI technology to be employed in reconfigurable optical systems.

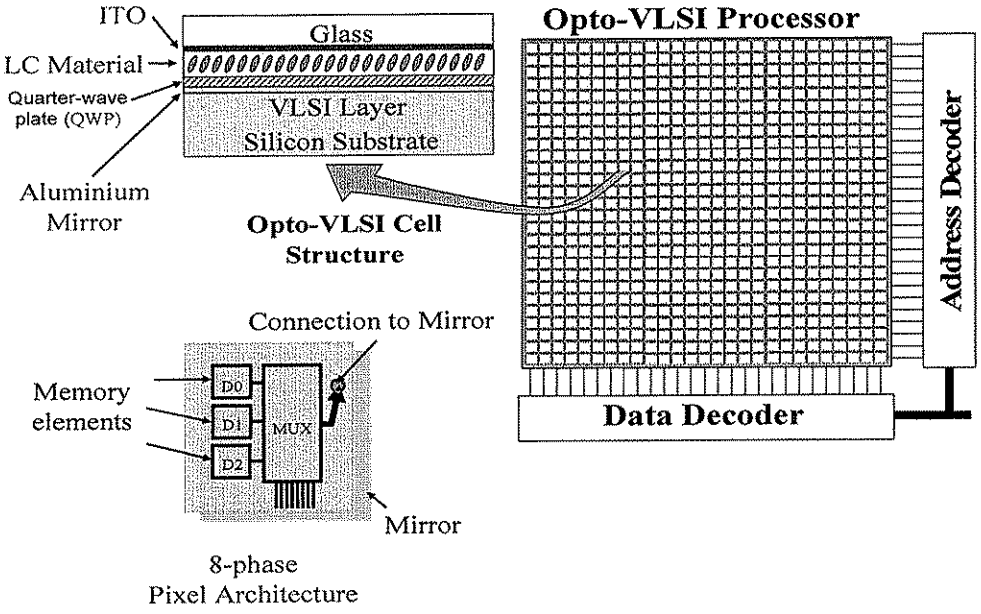

Fig. 1. Opto-VLSI processor and LC cell structure design.

Figure 2 illustrates the ability of an Opto-VLSI processor to perform beam steering and multicasting without moving parts using the digital phase holograms shown in Fig. 2(a). Beam steering is achieved by generating a digital blazed grating whose pitch can be varied by changing the voltage applied to each pixel. For a blazed grating of pitch q×d, the steering angle Θ is proportional to the wavelength (λ) of the light and inversely proportional to q×d, as shown in Fig. 2(b). On the other hand, a multicasting phase hologram can be loaded, which generates multiple beams of arbitrary intensities.

For a small incidence angle, the maximum steering angle of the Opto-VLSI processor is given by [21]:

$$\theta_{\max} \approx \frac{\lambda}{M \cdot d} \quad \text{(Radians)} \qquad (1)$$

Where M is the number of phase levels, d is the pixel size, and λ is the wavelength of the incident beam. For example, a 4-phase Opto-VLSI processor having a pixel size of 5 microns can steer a 1550 nm laser beam by a maximum angle of around ±4°. The maximum diffraction efficiency of an Opto-VLSI processor is given by [24]:

$$\eta = \mathrm{sinc}^2\left(\frac{\pi n}{M}\right) \qquad (2)$$

where $n = gM + 1$ is the diffraction order ($n = 1$ is the desired order), and g is an integer. According to Eqs (1) and (2), an Opto-VLSI processor with four phase levels allow for efficiency up to 81%. Note that, in the steering mode, the higher diffraction orders (which correspond to the cases $g \neq 0$) are usually unwanted crosstalk, which, through a proper design, can be attenuated or properly routed outside the output ports to maintain a high signal-to-crosstalk performance.

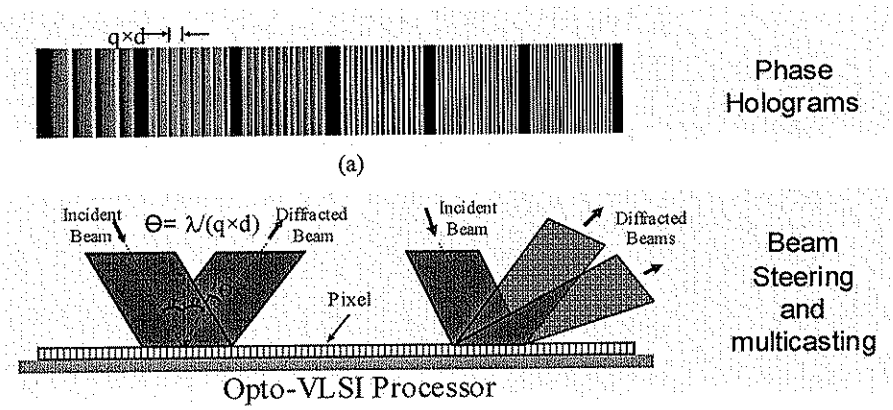

Fig. 2. (a) Phase holograms driving various pixel blocks, (b) Principle of beam steering and multicasting using an Opto-VLSI processor.

3. OPTICAL INTERCONNECT ARCHITECTURE

Figure 3 illustrates the concept for the reconfigurable optical interconnect structure [17], which employs VCSEL and photodetector arrays in conjunction with two Opto-VLSI processors mounted at 45° on an optical substrate covering the VCSEL and PDs arrays field of view to achieve dynamic beam steering with near normal incidence on the photodetector array.

The active window of each Opto-VLSI processor is divided into pixel blocks. Every pixel block on the first Opto-VLSI processor is assigned to a VCSEL element, whereas each pixel block on the second Opto-VLSI processor is assigned to a PD element. To establish an optical interconnect between a VCSEL element and a PD element, the assigned pixel blocks are loaded with proper steering holograms. The VCSEL's hologram generated on the first Opto-VLSI steers the VCSEL beam toward the PD's pixel block on the second Opto-VLSI processor. The PD's hologram generated on the second Opto-VLSI steers the optical beam to the PD element. Note that the maximum steering angle of the second Opto-VLSI processor determines the maximum number of optical interconnects that can be achieved. The optical been is collimated and focused using lens arrays.

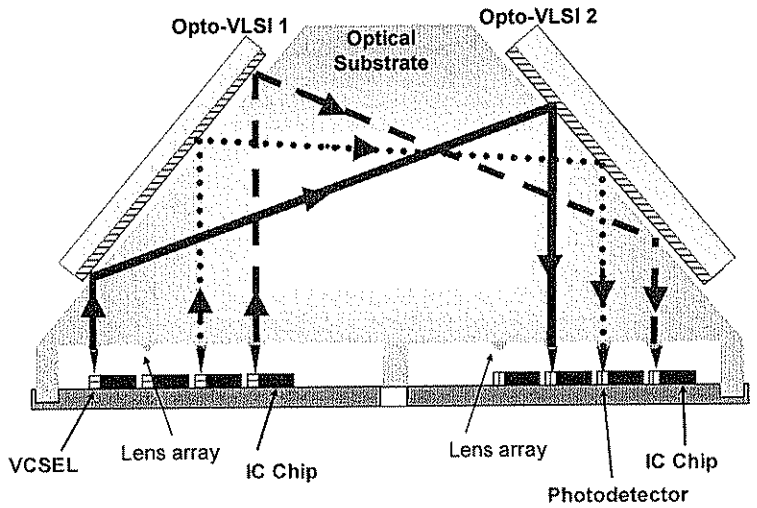

Fig. 3. Reconfigurable optical interconnects between the third VCSEL and any PD

4. EXPERIMENTAL SETUPS AND RESULTS

3.1 A single reconfigurable optical interconnect

Fig. 4 shows a setup where an 850nm VCSEL element modulated at 2.5Gbps was sequentially interconnected with three PD elements. For each optical interconnect, phase holograms were generated on the first Opto-VLSI processor to steer the VCSEL beam to different pixel blocks on the second Opto-VLSI processor, which are assigned to the different PD elements. Each of the PD pixel blocks was driven by an appropriate phase hologram that steered the optical beam towards its assigned PD element.

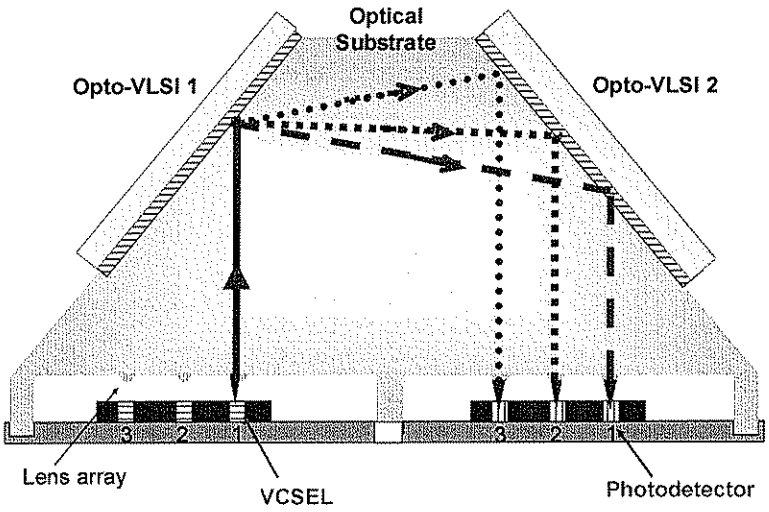

Fig. 4. Reconfigurable single optical interconnects.

Figures 5(a)-(c) show the sequential steering holograms that were used to drive the first Opto-VLSI processor to establish optical interconnects from the VCSEL element to the first, second, and third PD element, respectively. Figure 5(d) shows the phase holograms driving the second Opto-VLSI processor, which steer the VCSEL beams to the various PD elements.

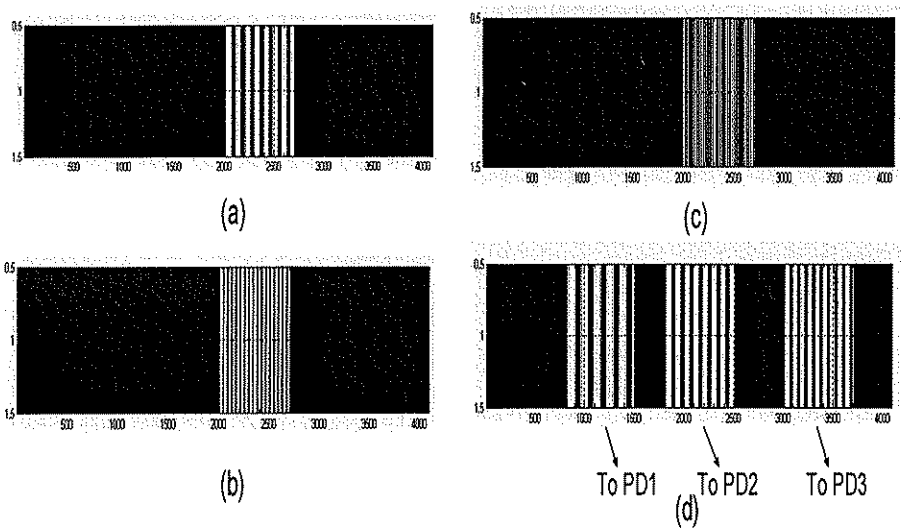

Fig. 5. Optimum steering holograms of the Opto-VLSI processors for establishing the different optical interconnects from the VCSEL element to any PD element.

A computer algorithm based on real-time optimisation was developed to generate the optimum phase holograms that maximise the signal at the output port of the intended optical interconnects. Figure 6 shows the output waveforms and eye diagrams for each interconnect. It is obvious that the output eye diagram openings are large and clear, implying that the received signal powers were adequate for further signal processing. Note that the thermal noise was the dominant noise source.

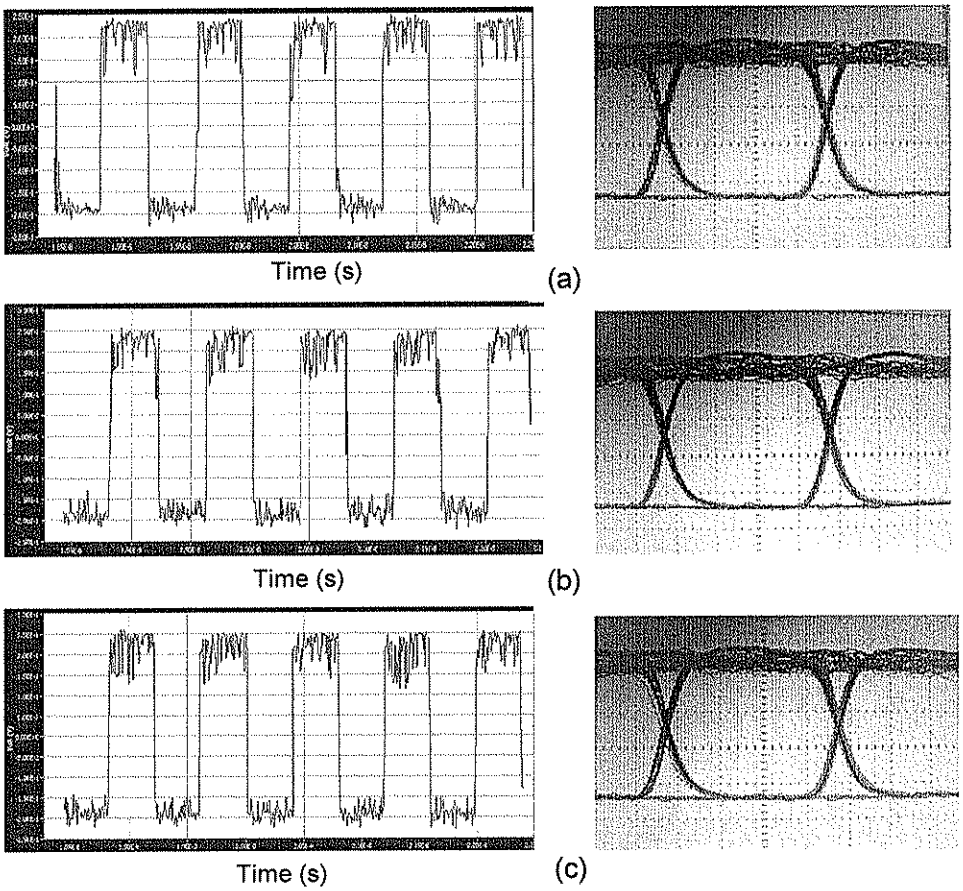

Fig. 6. Output signals and eye diagrams for optical interconnect between the VCSEL element and the (a) first (b) second and (c) third PD element.

3.2 Multicasting optical interconnects

Figure 7 shows a multicasting interconnect setup which was established between a VCSEL element and two PD elements. A multicasting hologram was generated on the first Opto-VLSI processor, which equally split the VCSEL beam into two beams, and route them toward the first and second PD pixel blocks. Figure 8 shows the multicasting phase hologram of the first Opto-VLSI processor as well as the steering phase holograms of the second Opto-VLSI processor. Figure 9 shows the detected optical signals and eye diagrams at the output ports of both optical interconnect. Note that in this case lower signal-to-noise ratios are observed in comparison to the interconnect scenario of Section 3.1. This is because of the inherent splitting loss associated with beam multicasting.

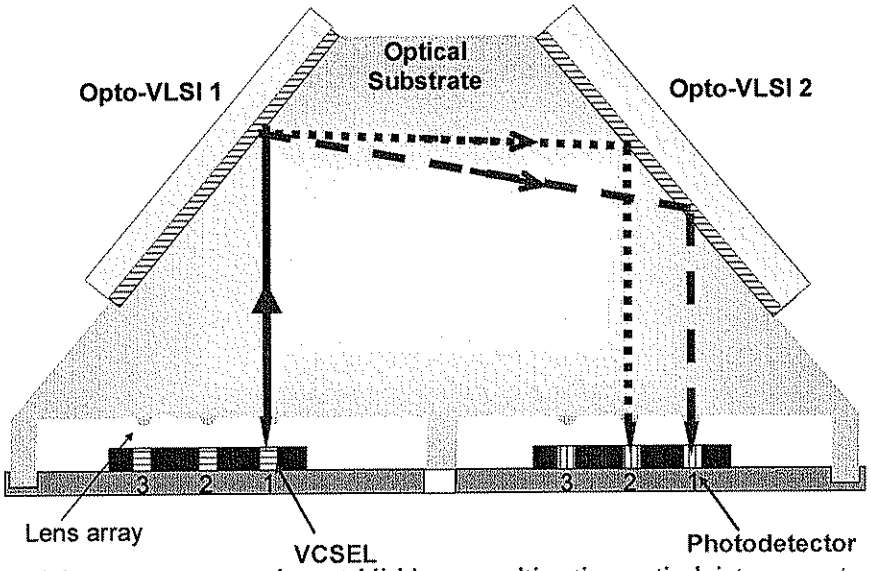

Fig. 7. Second interconnect scenario: establishing a multicasting optical interconnects between a VCSEL element and two PD elements.

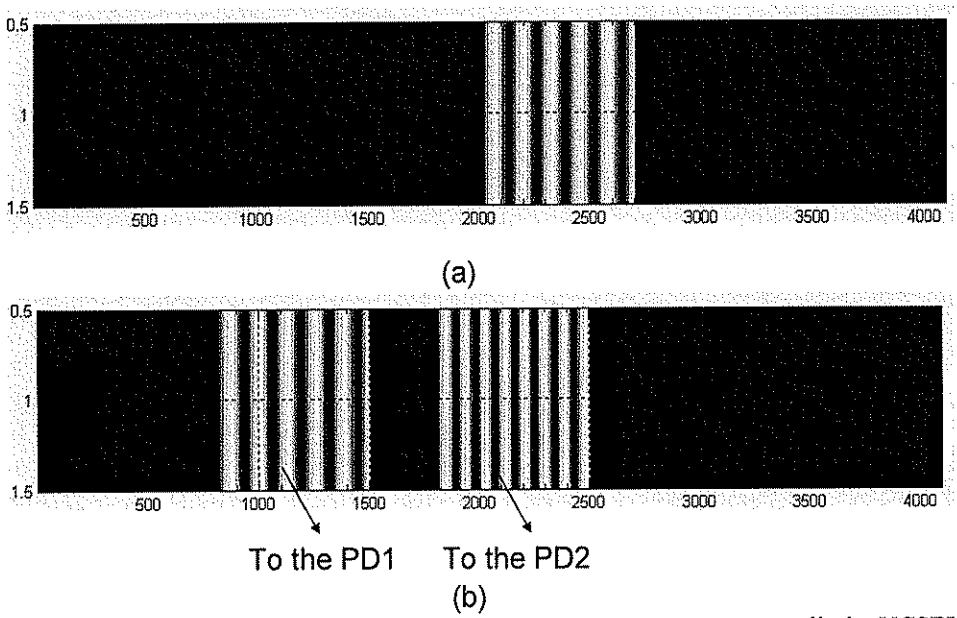

Fig. 8 (a) Multicasting hologram generated on the first Opto-VLSI processor to split the VCSEL beam towards the pixel blocks assigned to the first and the second PD elements on the second Opto-VLSI processor, (b) the steering holograms generated on the second Opto-VLSI processor to steer the optical beams to the first and the second PD elements.

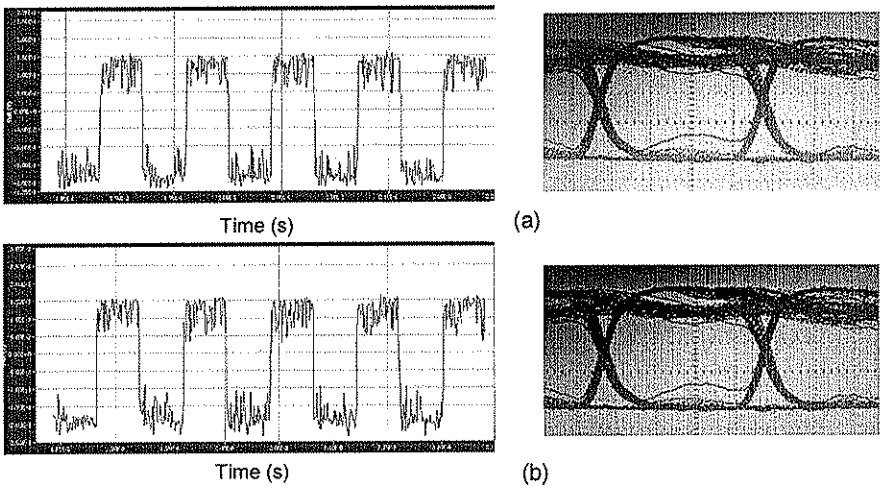

Fig. 9. Output signals and the eye diagrams at the output port of (a) the first PD element, and (b) the second PD element.

5. CONCLUSION

We have demonstrated a 2.5Gbps reconfigurable optical interconnects architecture constructed using an 850nm VCSEL array, a photodiode (PDs) array, and two Opto-VLSI processors. Each Opto-VLSI processor has been driven with a proper steering holograms. The proof of concepts has been demonstrated for point-to-point and multicasting scenarios. This architecture is attractive for reconfigurable chip-to-chip and board-to-board optical interconnects, and addresses future requirements for processor-memory and processor-processor communications.

REFERENCES

1. Cho. Hoyeol, P. Kapur, and K.C. Saraswat, "Power comparison between high-speed electrical and optical interconnects for interchip communication", *J. Lightwave Technol.* 22(9), 2021 – 2033 (2004).
2. F.-C. F. Tsai, C. J. O'Brien, N. S. Petrović, and A. D. Rakić, "Analysis of optical channel cross talk for free-space optical interconnects in the presence of higher-order transverse modes," *Appl. Opt.* 44(30), 6380-6387 (2005).
3. X. Wang, F. Kiamilev, G. C. Papen, J. Ekman, P. Gui, M. J. McFadden, J. C. Deroba, M. W. Haney, and C. Kuznia, "Performance-based adaptive power optimization for digital optical interconnects," *Appl. Opt.* 44(29), 6240-6252 (2005).
4. B. E. Lemoff, M. E. Ali, G. Panotopoulos, G. M. Flower, B. Madhavan, A. F. J. Levi, D.W. Dolfi "MAUI: enabling fiber-to-the-Processor with parallel multiwavelength optical interconnects," *J. Lightwave Technol.* 22(9), 2043 – 2054 (2004).
5. R. T. Chen, L. Lin, C. Choi, Y. J. Liu, B. Bihari, L. Wu, S. Tang, R. Wickman, B. Picor, M. K. Hibbs-brenner, J. Bristow, and Y. S. Liu, "Fully embedded board-level guided-wave optoelectronic interconnects," *Proc. IEEE*, 88, 780–793 (2000).
6. F. Mederer, R. Jager, H. J. Unold, R. Michalzik, K. J. Ebeling, S. Lehmacher, A. Neyer, and E. Griese, "3-Gb/s data transmission with GaAs VCSEL's over PCB integrated polymer waveguides," *IEEE Photon. Technol. Lett.* 13, 1032–1034 (2001).
7. Y. Li, J. Ai, and J. Popelek, "Board-level 2-D data-capable optical interconnect circuits using polymer fiber-image guides," *Proc. IEEE*. 88, 794–805 (2000).

8. T. May, A. G. Kirk, D. V. Plant, J. F. Ahadian, C. G. Fonstad, K. L. Lear, K. Tatah, M. S. Robinson, and J. A. Trezza, "Interconnection of a two-dimensional array of vertical-cavity surface-emitting lasers to a receiver array by means of a fiber image guide," *Appl. Opt.* 39(5), 683–689 (2000).
9. L. A. Buckman Windover, J. N. Simon, S. A. Rosenau, K. Giboney, G. M. Flower, L. W. Mirkarimi, A. Grot, B. Law, C. K. Lin, A. Tandon, R. W. Gruhlke, H. Xia, G. Rankin, and D. W. Dolfi, "Parallel Optical Interconnects Beyond > 100 Gb/s," *J. Lightwave Technol.* 22, 2055–2063 (2004).
10. H. F. Bare, F. Haas, D. A. Honey, D. Mikolas, H.G. Craighead, G. Pugh, R. Soave, "A simple surface-emitting LED array useful for developing free-space optical interconnect," *IEEE Photon. Technol. Lett.* 5(2), 172 – 175 (1993).
11. J. Jahns, Y. H. Lee, C. **A.** Burrus, and J. L. Jewell, "Optical interconnects using top-surface-emitting microlasers and planar optics," Appl. Opt. 31(5) 592-597 (1992).
12. D. V. Plant, M. B. Venditti, E. Laprise, J. Faucher, K. Razavi, M. Chateauneuf, A. G. Kirk, and J. S. Ahearn, "256-channel bidirectional optical interconnect using VCSEL's and photodiodes on CMOS," *J. Lightwave Technol.* 19, 1093–1103 (2001).
13. D.V. Plant, A.G. Kirk, "Optical interconnects at the chip and board level: challenges and solutions," *Proc. IEEE.* 88(6), 806 – 818 (2000).
14. R. Wang, A. D. Raki, and M. L. Majewski, "Design of Microchannel Free-Space Optical Interconnects Based on Vertical-Cavity Surface-Emitting Laser Arrays," Appl. Opt. 41(17), 3469-3478 (2002).
15. D. Fey, W. Erhard, M. Gruber, J. Jahns, H. Bartelt, G. Grimm, L. Hoppe, S. Sinzinger "Optical interconnects for neural and reconfigurable VLSI architectures," *Proc. IEEE.* 88(6), 838 – 848 (2000).
16. M. Aljada, K. E. Alameh, and K. Al-Begain, "Opto-VLSI-based Correlator Architecture for Multi-wavelength Optical Header Recognition" *J. Lightwave Technol.* 24(7), 2779-2785 (2006).
17. M. Aljada, K. E. Alameh, Y-T. Lee, and I-S Chung, "High-speed (2.5 Gbps) reconfigurable inter-chip optical interconnects using opto VLSI processors," *OSA optics express.* 14(15), 6823- 6836 (2006).