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Abstract

We investigate the design and performance of a reconfigurable optical interconnect structure based on vertical-cavity surface-emitting lasers (VCSEL), Opto-VLSI processors and photodetector arrays. We optimise a proof-of-concept 3-VCSEL-element structure that eliminates crosstalk caused by unwanted diffracted optical beams and show that a bit error rate (BER) of 10^{-17} is feasible at 3.2 Gbps for each channel.

1. Introduction

As the data rate in Application Specific Integrated Circuits (ASICs) increases, the need for very high speed interconnects for clock and data distribution between chips becomes more difficult using copper traces and low cost PCB materials, which suffer from $f^{1/2}$ skin-effect losses as well as dielectric absorption [1]. Recently, low-cost VCSEL arrays along with photodiode arrays have become available allowing high bit rate low loss optical interconnects. Reconfigurable optical interconnects allow system designers another degree of freedom for interconnecting multi-function chips, thereby reducing the number of very high speed I/O required.

Spatial Light Modulators (SLMs) based on Liquid Crystal on Silicon (LCOS) optical phased arrays [2] have been proposed as beam steerers for reconfigurable optical interconnects [3] and along with VCSELs and photodiode arrays allow the design of rugged low-power high speed interconnects. Since SLMs are generally polarization-sensitive devices accurate polarization control is crucial to minimise the optical losses in SLM-based reconfigurable optical interconnects.

Opto-VLSI processors are reflective LCOS pixellated spatial light modulators that incorporate a Quarter Wave Plate (QWP) between the reflective electrode and the liquid crystal layer to achieve polarization insensitive operations. However, when operating in the steering mode, Opto-VLSI processors generate unwanted diffraction orders which are the major potential sources of channel crosstalk in optical interconnects [2]. For high speed (>1 GHz) optical interconnects the BER must be below 10^{-17} in order to achieve acceptable MTBF rates [1]. This places stringent requirements on the maximum allowable crosstalk between the optically interconnected channels. It has been shown that by careful design of the collimating optics, diffraction effects can be neglected [4]. In this paper, we investigate the crosstalk of an integrated Opto-VLSI optical interconnect structure and optimise the VCSEL and photodetector spacings to minimise the crosstalk routed to undesired channels, and demonstrate that the system power budget can provide the BER required for high-speed optical interconnects.

2. Reconfigurable optical interconnect architecture

Figure 1 shows the basic concept for an integrated bilateral reconfigurable interconnect structure that employs VCSEL and photodetector arrays in conjunction with two Opto-VLSI processors mounted face to face at right angle on an optical substrate to achieve dynamic beam steering with near normal incidence on the photodetector array.

A stepped blazed grating generated on the active surface of an Opto-VLSI processor steers an input optical beam incident at 45° by an angle $\Theta_{steered}$ given by [2]:

$$\Theta_{steered} = \arcsin\left[(m\lambda/qd) - \sin(45^\circ)\right] \qquad (1)$$

where

m = $0, \pm1, \pm2$ = diffraction order
λ = wavelength
q = blazed grating period in number of pixels ($10 < q < 128$)
d = pixel spacing

For a stepped blazed grating, the dominant diffraction orders are the zeroth and (±1) orders, of which the (+1) order beam is the wanted signal and the zeroth order (unsteered) along with the (-1) order beam are the dominant sources of unwanted crosstalk, which can significantly degrade the performance of the optical interconnects if not routed outside the active areas of the photodetector elements.

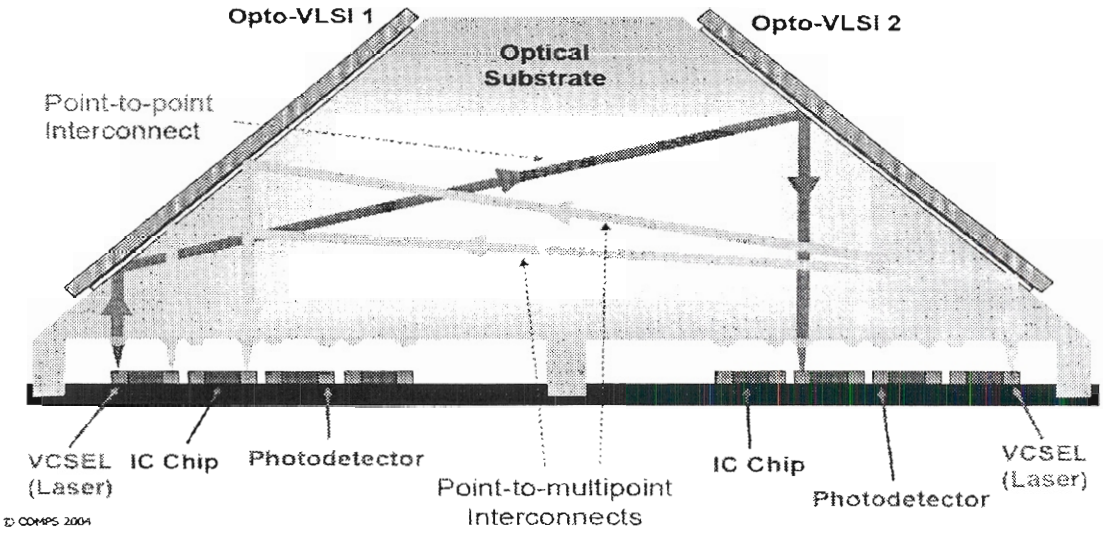

Figure 1. Configurable optical interconnect concept

Figure 2 shows the propagation of the zeroth and (±1) order beams within the optical interconnect structure. By offsetting the position of the photodetector elements and changing the photodetector spacing relative to the VCSEL element separations, the crosstalk from the overlapping between the zeroth order beams and the active areas of the photodetector elements can be made negligible, as illustrated in Figure 2. By introducing asymmetry in the VCSEL spacing, the crosstalk from unwanted steered beams can also be suppressed.

The minimum spacing between the VCSEL elements in our design is 500 μm and this allows for a maximum collimating microlens diameter, D, of 500 μm. To minimise the diffraction loss of the collimating lens, the collimated beam diameter, 2ω, must be kept below $\sqrt{2}D/3$ = 240 μm [4]. This sets the Rayleigh range (maximum working distance) to $Z_R = \pi \omega^2/\lambda$ = 53 mm, where λ is the VCSEL wavelength (850 nm).

3. Modelling of multi-beam propagation and optimisation of structure geometry

The major design parameters used for modelling the performance of the proposed optical interconnect structure shown in Figure 2 are the spacings between the VCSEL elements (d_1, d_2), the spacing between the photodetector elements, the maximum steering angle of the Opto-VLSI processors, and the maximum size of the structure (L_1, L_2). Since the array of photodetectors is illuminated by a multitude of beams originating from the diffraction orders of Opto-VLSI processors, the principal design challenge for this system is to minimise the crosstalk between the various interconnected channels. This is achieved through the routing of the unwanted optical beams outside the active areas of the photodetector elements, for all possible interconnection scenarios. The analysis and simulation of optical beam routing was performed using a C++ computer algorithm developed especially for the visualisation of beam propagation through the calculation of the coordinates of beam paths and their intersections with the plane of photodetectors. The calculations take into account all system parameters, including the geometry, steering angles (3.5° maximum for the Opto-VLSI processors), collimated beam diameters and Gaussian beam propagation.

The main objective of system design was to explore all interconnection scenarios and optimise the steering angles at both Opto-VLSI processors that minimise the crosstalk at the photodetectors. Another objective was to optimise the locations of the VCSEL and photodetector elements, which ensure steering to all possible interconnection scenarios. The modelling software represents beams incident on the detector array and ranges of signal beams steering for an arbitrary chosen combination of steering angles applied to the first Opto-VLSI processor and calculates the coordinates of the centre and edges of each beam path. As we stated in Section 2, the modelling was limited to the propagation of the dominant zeroth and (±1) diffraction orders generated by Opto-VLSI processors.

For a 3×3 optical interconnect structure, there are six switching states that cover all possible VCSEL/photodetector interconnect combinations. We represent each interconnection state using the following index notation: a state (x, y, z) describing the VCSEL-photodetector connection where a signal from VCSEL 1 reaches detector x, a signal from VCSEL 2 reaches detector y, and VCSEL 3 illuminates detector z, where x, y and z are detector numbers ranging from 1 to 3. Using this notation, the design of the interconnect system can be represented by a table of steering angles generated by the first Opto-VLSI processor for each state to ensure the ability of the second Opto-VLSI processor to steer all beams to their corresponding photodetectors without crosstalk.

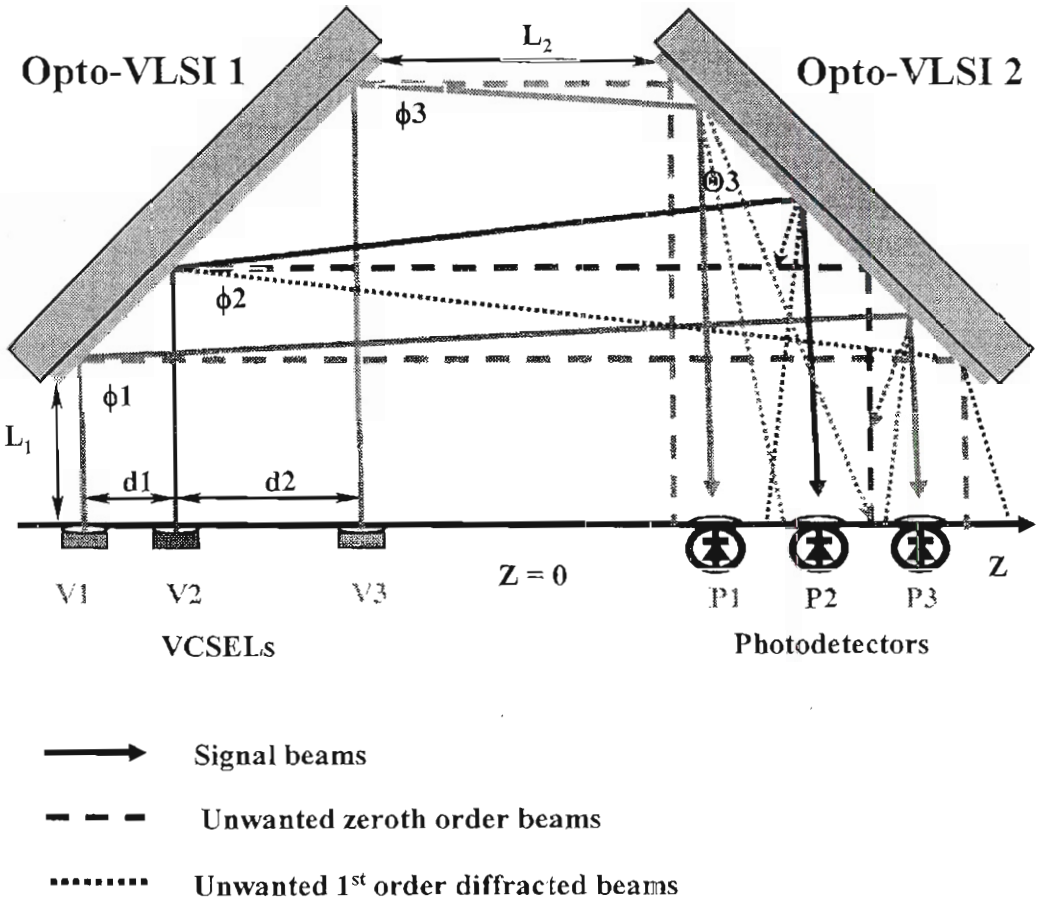

Figure 2. Propagation of zeroth and (±1) order beams within the proposed optical interconnect structure

A significant design consideration limiting the choice of possible VCSEL/photoreceiver locations and steering angles applied by the first Opto-VLSI processor is avoidance of cross-modulation effects arising from potential overlapping of signal beams with unused beams at the surface of the second Opto-VLSI processor, which can lead to the production of unwanted extra diffraction orders along the unused beam directions. To exclude cross-modulation, the positions of all beams at the second Opto-VLSI processor were modelled for all interconnection scenarios, and the optimisation took into account the cross-modulation effects to ensure sufficient separation of modulated and unmodulated regions across the second Opto-VLSI processor.

The following table represents the system design modelled with geometric parameters L_1 = 5 mm, L_2 = 40 mm, length of the Opto-VLSI processor L = 7 mm, VCSEL separations d_1 = 2 mm, d_2 = 0.5 mm, and photodetector coordinates z(P1) = 21.25 mm, z(P2) = 23 mm, z(P3) = 24 mm. The separations of VCSEL and photodetectors are quantised in 0.25 mm steps. The maximum working distance for the signal beams in this design does not exceed 60 mm, which is greater than the Rayleigh range by about 20 %.

Table 1. Switching state - steering angle matrix

Switching states	$\phi 1$ (degrees)	$\phi 2$ (degrees)	$\phi 3$ (degrees)
(1, 2, 3)	3.5	0.4	2.4
(1, 3, 2)	3.5	2	1.3
(2, 1, 3)	1.8	1.1	2.4
(2, 3, 1)	1.7	2	0.3
(3, 2, 1)	0.3	0.4	0.3
(3, 1, 2)	0.3	1.1	1.4

Figure 3 illustrates the state (1, 2, 3) and shows the distribution of beams incident at the photodetector array. The numbers at the different peaks indicate the VCSEL element from which the beams originate. The heights of the plotted "beams" do not represent their intensities, but are chosen to indicate the diffraction order of each beam. Here, the highest peaks represent locations and sizes of beams originating from the (+1) orders of the first Opto-VLSI processor after their zero-order reflection off the surface of the second Opto-VLSI processor. These beams are always present in the system, even if no modulation is applied to the second Opto-VLSI processor. When these (+1) order beams are steered for interconnection, they are further diffracted into (+1) and (-1) orders at the second Opto-VLSI processor. These

beams are not shown explicitly in Figure 3, however, the steering ranges for the locations of beams generated by the second Opto-VLSI processor are shown using the horizontal bars.

Similarly, the smallest peaks represent locations and sizes of beams originating from the (-1) orders of the first Opto-VLSI processor after their zero-order reflection off the surface of the second Opto-VLSI processor and the medium-sized peaks represent the fixed zero-order reflections of source beams. The latter are always present in the system at the same locations irrespective of applying any modulation signals. Finally, the black stripes represent the locations and widths of receiver lenses.

In order to steer light from VCSEL 1 onto Receiver 1 (located at z = 21.25 mm), the first order (+1) of diffraction at the first Opto-VLSI processor is used, which needs to be slightly steered (by some angle θ_1 not represented in graphs) using the second Opto-VLSI processor to provide maximum overlap at the receiver lens. When the second Opto-VLSI processor is used to steer beams it generates its own (+1), 0 and (-1) orders and their range is represented by the horizontal bar.

To steer light from VCSEL 2 onto Receiver 2, the (-1) order of diffraction at the first Opto-VLSI processor is used, with the corresponding receiver being in the steerable range for this beam, provided there is some further steering of the beam by the second Opto-VLSI processor. For directing light of VCSEL 3 onto Receiver 3, we use the (-1) order of diffraction at the first Opto-VLSI processor. Similarly, the receiver is located within the steering range for that beam.

Figure 4 illustrates the state (3, 2, 1) of the interconnect realised by using our modelled data. Here, a different set of diffraction orders generated by the first Opto-VLSI processor is used for signal delivery. For example, in order to reach Receiver 1 by light from VCSEL 3, its (+1) order of diffraction at the first Opto-VLSI processor is used. The graphs show that no overlapping with unwanted beams exists at all receiver locations within the Gaussian beam envelopes limited in width by one standard deviation.

We have modelled all of the six possible states and determined acceptably low crosstalk from unwanted Gaussian beam tails at the photodetectors for the geometry defined above. Modelling of interconnect systems with further degree of miniaturisation and investigation of the possibility of increasing the numbers of signal channels is an ongoing research.

4. Power budget

A given bit error rate (BER) performance determines the minimum system signal-to-noise ratio (SNR), and hence the minimum received optical power once the system noise has been determined. Knowing the maximum launched optical power and the system optical losses allows the estimation of the system margin. For board level interconnects, the BER must be much higher than that used in optical transmission systems, where error detection and subsequent packet re-transmission protocols are used. For board level interconnects operating at several Gbps, a BER of 10^{-17} is required [1]. The BER is given by [5]:

$$BER = \frac{1}{2}\left(erfc\left(\frac{Q}{\sqrt{2}}\right)\right) \qquad (2)$$

where $Q = SNR_{opt}$ is the optical SNR when the decision threshold is set optimally. According to (2), BER $=10^{-17}$ for $Q = 8.5$.

For the case where the photodetector is a PIN diode with responsivity, $\Re$ the thermal noise is dominant and equal for both the power in a ZERO bit, P_0 and the power in a ONE bit, P_1, SNR_{opt} is given by:

$$SNR_{opt} = \Re\left(P_0 - P_1\right)/2i_{eq} = \Re\frac{P_{\min}}{i_{eq}}\frac{\left(r_e - 1\right)}{\left(r_e + 1\right)} \qquad (3)$$

where P_{min} is the minimum average received optical power, and i_{eq} is the RMS equivalent input noise current for the transimpedance amplifier, and r_e is the extinction ratio given by (P_1/P_0).

For the usual case where the amplifier with transimpedance R_f is followed by a limiting amplifier, another factor relating to the limiting amplifier's minimum sensitivity, V_{th} must be included, yielding [6]:

$$P_{\min} = \frac{1}{\Re}\left[i_{eq}\,SNR_{opt} + \frac{V_{th}}{R_f}\right]\frac{\left(r_e + 1\right)}{\left(r_e - 1\right)} \qquad (4)$$

For a MAXIM-3725 3.2 Gbps transimpedance amplifier, the input equivalent noise in a 2.1 GHz bandwidth is 325 nA and R_f is 3.5 kΩ typically. For a limiting amplifier with input sensitivity of 5 mV, an extinction ratio of 10, and a responsivity of 0.5 A/W, we get:

$P_{min} = 10.2\ \mu W$
$= -19.9$ dBm

The maximum launched power for a single-mode VCSEL is taken as 1 dBm, and the VCSEL relative intensity noise (RIN) is assumed to be -150 dB/Hz [7]. For such low values of RIN, the power penalty due to RIN is negligible [8].

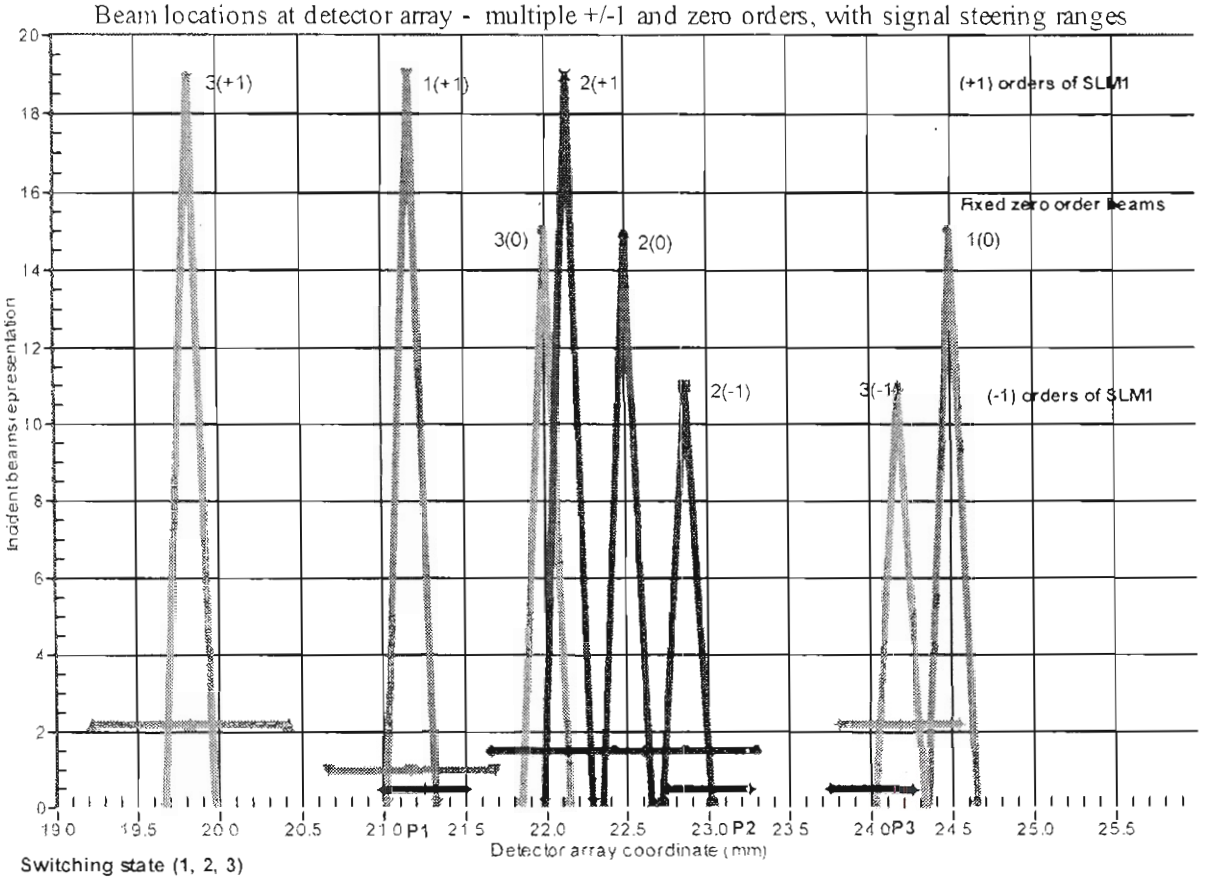

Figure 3. Modelled distribution of beams illuminating the photodetector array during the switching condition (V1 → P1, V2 → P2, V3 → P3)

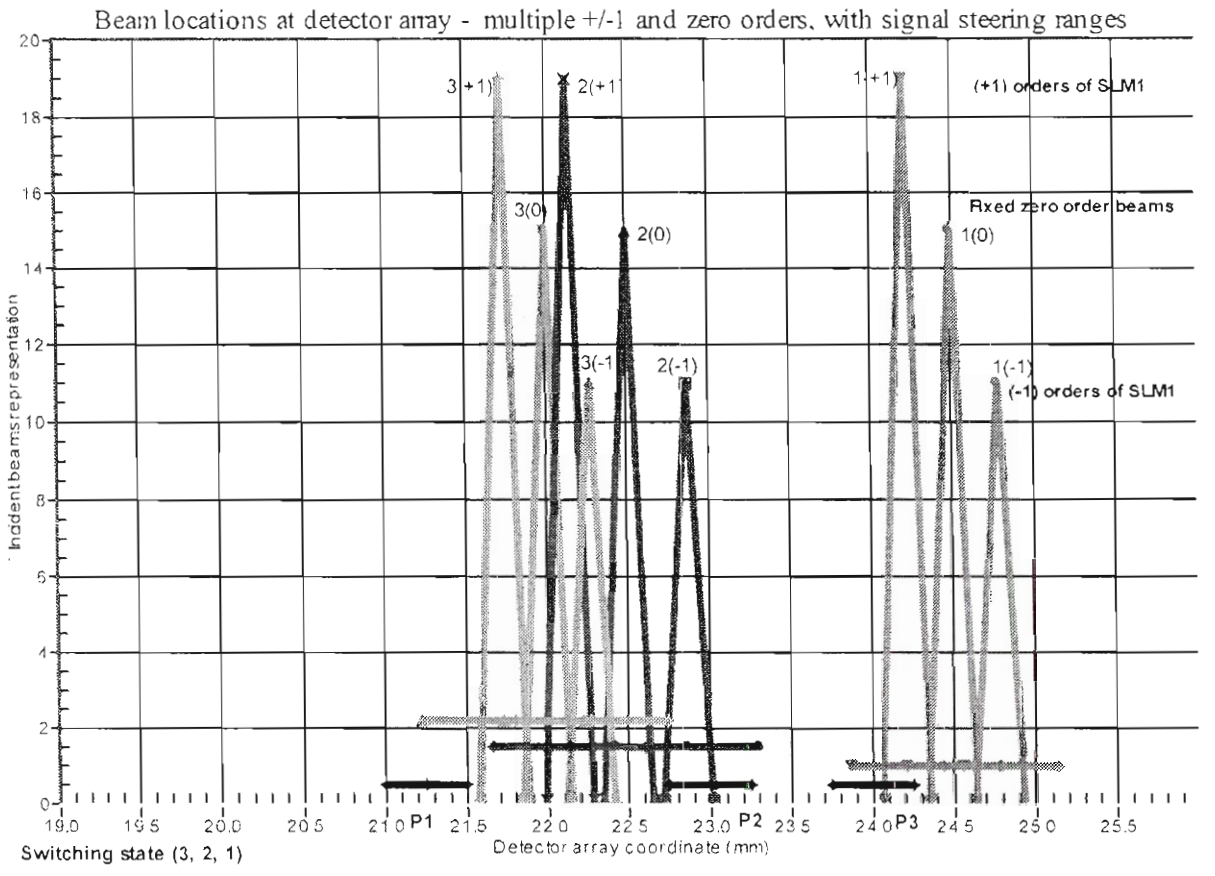

Figure 4. Modelled distribution of beams illuminating the photodetector array for various switching scenarios (V1 → P3, V2 → P2, V3 → P1)

Table 2 shows the system losses and required system margins for a BER of 10^{-17}.

Table 2. System power budget

System Parameter	
Laser output power	+1 dBm
Laser collimating and coupling loss	-2 dBm
Opto-VLSI processor loss (x2)	-10 dBm
Power Incident at detector	**-11 dBm**
Inter Symbol Interference margin	-1 dBm
Power Rail degradation	-2 dBm
Laser Diode EOL margin	-1 dBm
Total Margin	**-4 dBm**
Available Margin	**19.9 – 15 = 4.9 dB**

As shown in Table 2, we have taken into account optical losses arising from the collimating optics and typical Opto-VLSI processor losses obtained from measurements. Furthermore, we have allowed margins for typical impairments such as laser end-of-life (EOL) degradation and power rail noise [1]. The resulting available margin of 4.9 dB gives sufficient head-room to ensure a robust interconnect solution.

5. Conclusions

We have analysed and modelled an integrated reconfigurable interconnect using two Opto-VLSI processors and designed for operation at 3.2 Gbps per channel. Our model shows the Gaussian beam profiles due to wanted and unwanted diffracted and reflected beams, taking beam divergence into account. The analysis has allowed the optimisation of the position of VCSEL sources and photodetectors that minimise crosstalk to a sufficiently low level thus achieving our target BER. A detailed link power budget analysis has shown that for a BER = 10^{-17}, a high system margin of 4.9 dB can be attained with a single-mode, +1 dBm VCSEL source.

6. References

[1] D. H. Hartman, "Optical interconnection technology in the telecommunications network", *IEEE Proc.* 1986 ACM Fall Joint Computer Conference, 1986.

[2] P. F. McManamon et al, "Optical phased array technology", *IEEE Proc.* Vol 84, No. 2, Feb. 1996.

[3] W. Heirman et al, "Traffic temporal analysis for reconfigurable interconnects in shared-memory systems", *Proc. 15th ProRISC Workshop*, Technology Foundation STW, pp. 39-44, 2004.

[4] R. Wang, A. D. Rakic and M. L. Majewski, "Design of microchannel free-space optical interconnects based on vertical-cavity surface-emitting laser arrays", *Applied Optics*, Vol. 41, No. 17, June, 2002.

[5] S. D. Personick, "Receiver design for digital fiber optic communication systems", *BSTJ*, Vol. 53, No. 6, July-August, 1973.

[6] Maxim, *"Accurately estimating optical receiver sensitivity"*, HFAN-3.0.0, Rev 0; 6/01.

[7] D. Wiedenmann et al, "Noise characteristics of 850 nm single-mode vertical cavity surface emitting lasers", *Applied Physics Letters*, Vol. 73, Issue 6, August 10, 1998.

[8] S. Kanprachar, "*Modeling and Analysis of the Effects of Impairments in Fiber Optic Links*", MSc Thesis, Virginia Polytechnic Institute and State University, September, 1999.