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Image Capture Using Integrated 3D SoftChip Technology

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Abstract

Mobile multimedia communication has rapidly become a significant area of research and development constantly challenging boundaries on a variety of technological fronts. The processing requirements for the capture, conversion, compression, decompression, enhancement, display, etc. of increasingly higher quality multimedia content places heavy demands even on current ULSI (ultra large scale integration) systems, particularly for mobile applications where area and power are primary considerations. The system presented in this paper is designed as a vertically integrated (3D) system comprising two distinct layers bonded together using Indium bump technology. The top layer is a CMOS imaging array containing analog-to-digital converters, and a buffer memory. The bottom layer takes the form of a configurable array processor (CAP), a highly parallel array of soft programmable processors capable of carrying out complex processing tasks directly on data stored in the top plane. Until recently, the dominant format of data in imaging devices has been analog. The analog photocurrent or sampled voltage is transferred to the ADC via a column or a column/row bus. In the proposed system, an array of analog-to-digital converters is distributed, so that a one-bit cell is associated with one sensor. The analog-to-digital converters are algorithmic current-mode converters. Eight such cells are cascaded to form an 8-bit converter. Additionally, each photosensor is equipped with a current memory cell, and multiple conversions are performed with scaled values of the photocurrent for colour processing.

1 Introduction

In the span of a few years, mobile multimedia communication has rapidly become a significant area of research and development constantly challenging boundaries on a variety of technological fronts. The pending roll-out of the 3G (3rd generation) and 4G (4th generation) wireless communications networks is further driving this development with the expectation for ever increasing levels of media rich content. The processing requirements for the capture, conversion, compression, decompression, enhancement, display, etc. of increasingly higher quality multimedia content places heavy demands even on current ULSI (ultra large scale integration) systems, particularly for mobile applications where area and power are primary considerations. In order to fully realise the capabilities promised by the 3G and 4G networks new enabling technologies are needed to facilitate the next generation of personal communications devices [1, 2]. In addition to the requirements for very low power, compact size and real-time processing, the rapidly evolving nature of telecommunications networks means that flexible soft programmable systems capable of adaptation to support a number of different standards and/or roles in the overall mobile communication system become highly desirable.

Although fully software driven solutions for these problems could be developed, it is unlikely within current technological limitations that such solutions would be able to meet the requirements for very low power real-time processing.

The proposed system is designed as a vertically integrated (3D) system [3] comprising two distinct layers. The top layer takes the form of a transducer array, in this case a CMOS imaging array. Additionally this array will include a massively parallel, interconnected frame/state buffer memory allowing for very high speed data manipulation within the plane. Current active pixel sensors (APS) are focused on front-illuminated architectures, where the sensors and the signal processing circuitry are integrated in the same plane. The main feature of the APS concept is that each pixel includes a photosensor and a read-out circuit, which processes the photocurrent or photovoltage. To increase the fill-factor and thus the spatial resolution the die area used for a sensor should be maximized leaving a very limited space for the circuitry. Up till now the dominant format of data in imaging devices is still analog. The analog photocurrent or sampled voltage is transferred to the ADC via a column or a column/row bus. The first fully digital pixels have been reported in [4,5,6,7]. The pixels from [4,6,7] are characterized by very low fill factor and

relatively high pitch as the amount of circuitry required is significantly larger than in the case of the APS. However, the pixel level A/D conversion potentially offers higher SNR than chip or column level A/D conversion, and a dramatic reduction of power dissipation, brought about as a result of parallelizing the processing and reducing the clock speed [5]. In the proposed system, an array of analog-to-digital converters is distributed, such that a one-bit cell is associated with each sensor. The analog-to-digital converters are algorithmic current-mode converters. Eight such cells are cascaded to form a full 8-bit converter. Additionally, each photosensor is equipped with a current memory cell, and multiple conversions are performed with scaled values of the stored photocurrent for colour processing.

The bottom layer will take the form of a configurable array processor (CAP), a highly parallel array of soft programmable processors capable of carrying out complex processing tasks directly on data stored in the top plane via Indium bump interconnects [8,9]. Each of these processors includes its own embedded memory, along with a high precision ALU and instruction decoder. Software programmed instructions are sent globally to all processors from separate on-chip RAM. Transforms and other processing (e.g. modified discrete cosine transform, motion estimation, edge detection, etc.) are then carried out according to these software instructions on the highly parallel array allowing for very high speed data manipulation and throughput at low clock speed. A high efficiency bus architecture is implemented to interconnect the parallel array processors for rapid extraction or insertion of data. The resulting system is very flexible due to the programmable nature of the CAP and very efficient due to the vertical interconnects and parallelization and thus theoretically very low power, yet capable of highly complex real-time processing tasks. These features make the system ideal for mobile multimedia type applications and, as all components are based on standard CMOS technologies, it should also be suitable for low cost consumer products.

This paper details the architecture of the top level sensor array concentrating on the design and performance of the analog-to-digital converter array.

2 Indium bump technology

The Indium bump technology allows the realization of a system comprising two CMOS chips, as shown in Figure 1. The upper layer – the “seeing” chip, contains an array of photodetectors and AD converters, the lower one – the “processing” chip, includes the low power configurable array processor, as shown in Figure 2.

As the chips are bonded face-to-face, it is not possible to conventionally illuminate the “seeing” chip from the front side, but only from the backside of the chip. To achieve this it is thinned by silicon bulk micromachining to approximately 150 – 300 μm . Using anisotropic etching the wafer is further thinned to the final thickness of several microns.

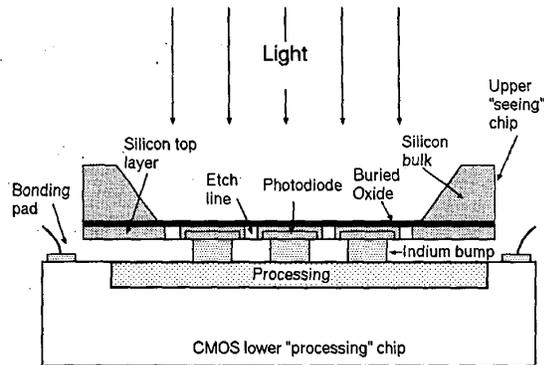


Figure 1 Two chips bonded by means of Indium bumps

The pixel pitch, determined by the current capabilities of Indium bump technology, is approximately 20 μm . However, the actual pixel size in the proposed system is larger than the minimum – approximately 50 $\mu\text{m} \times 50 \mu\text{m}$, so that the sensor and the additional circuitry in the top layer can be accommodated in 0.18 μm technology.

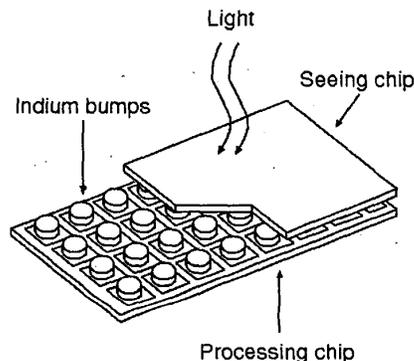


Figure 2 Physical construction of the array

3 The seeing chip architecture

The top level chip is a sensor array containing the sensor itself, analog-to-digital converters, and a buffer memory as presented in Figure 3.

The high-accuracy current memory cell used can be found in [13] and is depicted in Figure 3(b).

A standard RRGB Bayer pattern filter is applied over the photodiode array for full colour capture. For conversion to YCrCb colour-space the captured R, G or B values in each pixel must be appropriately weighted and interpolated. The scaling is realized using current mirror scaling circuits prior to A/D conversion. The appropriately scaled values from R, G and B pixels can then be interpolated to their Y, Cr or Cb equivalents using a simple digital manipulation. The analog current copier storage cell allows the interpolation/conversion for

each of these colour components to be carried out sequentially without any requirement for additional digital storage.

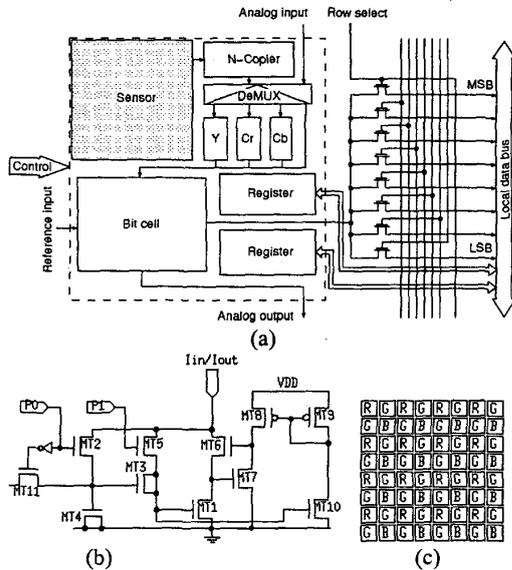


Figure 3 Image capture layer architecture:
 (a) The pixel structure
 (b) Current memory cell
 (c) RGGB Bayer pattern

4 Distributed algorithmic current-mode analog-to-digital converter

4.1 General structure

Current-mode algorithmic analog-to-digital converters are characterized by a very small amount of silicon area required and relatively simple hardware. A block diagram of the 1-bit converter is shown in Figure 4. The circuit operates as follows. The input current I_{in} is first multiplied by 2 and then compared with the reference current I_{ref} . If the signal $2I_{in}$ is less than I_{ref} the digital output goes low and an output current $2I_{in}$ is produced. However, if $2I_{in}$ exceeds I_{ref} , the digital output goes high, the switch will be closed and an output current of $2I_{in} - I_{ref}$ is produced. An N-bit converter is obtained by cascading N 1-bit cells connecting the analog output with the analog input of the following cell.

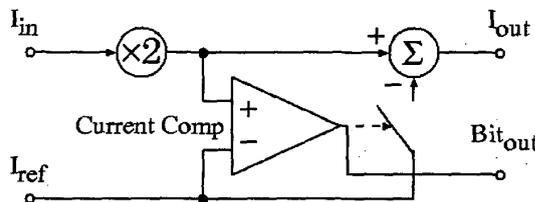


Figure 4 A bit cell for one bit A/D algorithmic conversion

An implementation of the above scheme using simple current mirrors, cascoded mirrors as well as active mirrors has been presented by Nairn et al. in [10,11]. It has been demonstrated that in the simple implementation, the accuracy of the subtracting block is the primary source of error, especially if the input current I_{in} is very close to the I_{ref} . The cascoded mirror implementation solves this problem, but the consequent reduction of the dynamic range of the $\times 2$ block is detrimental, and to achieve the same 8-bit accuracy the supply voltage needs to be increased.

One highly advantageous property of this type of converter is the absence of control signals. No external lines are required except for the input current and reference voltage, output digital bit lines and the power supply.

4.2 Regulated cascode mirror implementation

An implementation of the algorithmic 1-bit converter from Figure 3, using regulated cascode current mirrors is shown in Figure 5(a). Figure 5(b) presents the generation of the reference signal to be distributed for all one-bit cells.

The negative feedback in the regulated cascode mirrors provides an extremely high output resistance and also a small minimum output voltage (for the n-type mirror), which is equal approximately to a single saturation voltage of the transistor. This allows the use of such mirrors effectively in submicron technologies where the transistor output resistance in saturation and the power supply voltage are relatively low. Moreover, the transistors do not need to be very long, as opposed to the case of the simple mirror implementation where the transistor length is used to achieve high output resistance. However, the gate area must still be kept relatively large for sufficient V_T matching.

The current comparator in the converter is implemented as a cascade of two inverters where the first inverter operates as an integrating current-to-voltage converter providing filtering of the power supply noise.

The converter combines the advantage of precision subtraction of cascode mirrors with the high dynamic range of simple mirrors. It is also worth noting that the converter does not use any capacitors, linear or MOS, and the components used are fully compatible with a standard digital process.

4.3 Distributed converter architecture

Eight active bit-cells form a distributed A/D converter and each bit cell in the array can remain in one of the three states: selected cell, subordinate cell or inactive cell. In addition to the single-bit cell from Figure 4, the pixel requires configuration circuitry to enable the formation of the 8-bit cascade, sliding down the array according to the row select signal. In the selected cell the input current is

the sensor allowing for a significant reduction of the speed required for the scanning process. Moreover, there is very little switching, compared with the existing pixel-level AD converters employing counting and/or oversampling, yielding very low power dissipation for the sensor array. Further work will include the noise analysis of the proposed converter architecture and verification of the results obtained from simulation against the data obtained from the experimental chip planned for fabrication in mid-2002.

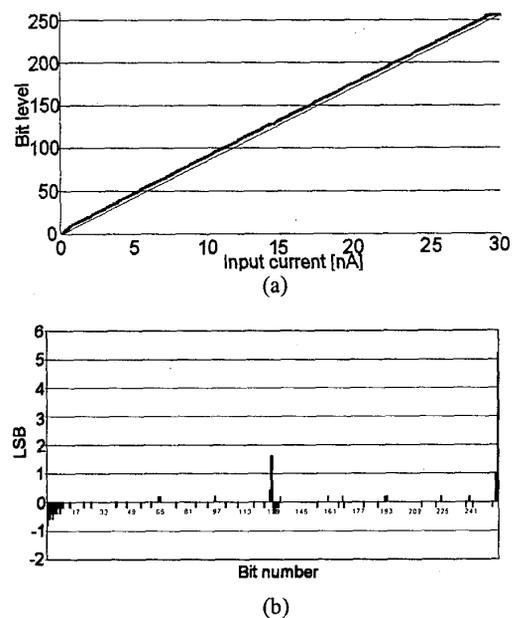


Figure 7 Operation of the converter simulated in UMC018 technology.
 (a) transfer characteristic
 (b) differential nonlinearity

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